Elmore Routing Tree (ERT) Algorithm

- Perform ERT algorithm under 65nm technology
  - Unit-length resistance $r = 0.4 \ \Omega/\mu m$
  - Unit-length capacitance $c = 0.2 \ f F/\mu m$
  - Driver output resistance $r_d = 250 \ \Omega$
  - Sink input capacitance $r = 50 \ f F$
Adding First Edge

- Simply add the nearest neighbor to the source
  - Add $(s,a)$
Adding Second Edge

- Rule: each node in $T$ can connect to its nearest neighbor
  - Two edges to consider: $(a,b), (s,c)$
  - Elmore delay calculations shown on next slides

![Diagram](image)
Elmore Delay Calculation

- Case 1: edge \((a,b)\)

\[
\begin{align*}
t(b) &= r_d \cdot C_s + r_{(s,a)}(0.5c_{(s,a)} + C_a) + r_{(a,b)}(0.5c_{(a,b)} + z_b) \\
&= r_d \cdot (c_{(s,a)} + z_a + c_{(a,b)} + z_b) + r_{(s,a)}(0.5c_{(s,a)} + z_a \\
&\quad + c_{(a,b)} + z_b) + r_{(a,b)}(0.5c_{(a,b)} + z_b) \\
&= 0.25(600 + 50 + 1200 + 50) + 1.2(300 + 50 + 1200 \\
&\quad + 50) + 2.4(600 + 50) \\
&= 3955ps
\end{align*}
\]
Elmore Delay Calculation (cont)

- Case 2: edge $(s,c)$
  - It is easy to see that $t(c) > t(a)$
  - Elmore delay is $t(c) = 2035\text{ps}$
  - Thus, we add $(s,c)$ to minimize maximum Elmore delay
Adding Third Edge

- Three edges to consider: \((a,b), (s,d), (c,d)\)
  - Elmore delay: \(t(b) = 4267.5\)ps, \(t(d) = 2937.5\)ps, \(t(d) = 5917.5\)ps
  - Add \((s,d)\)

\[
t(c) = 2937.5\text{ps}
\]
Adding Fourth Edge

- Four edges to consider: \((a,b), (s,b), (c,b), (d,b)\)
  - In all these cases, delay to \(b\) is the maximum
  - \(t(b) = 4630\,\text{ps}, 4720\,\text{ps}, 10720\,\text{ps}, 8310\,\text{ps}\), respectively
  - Add \((a,b)\)
Final ERT Result

- Maximum Elmore delay is \( t(b) = 4630 \text{ps} \)
  - No Steiner node used
  - Star-shaped topology
**Steiner Elmore Routing Tree (SERT)**

- Perform SERT algorithm under $1.2\mu m$ technology
  - Unit-length resistance $r = 0.073 \, \Omega/\mu m$
  - Unit-length capacitance $c = 0.083 \, fF/\mu m$
  - Driver output resistance $r_d = 212 \, \Omega$
  - Sink input capacitance $r = 7.1 \, fF$
First Iteration

- Simply add the nearest neighbor to the source
  - Add \((s,a)\)
Second Iteration

- Rule: each node not in $T$ can connect to each edge in $T$ using a Steiner point or directly to source
  - 6 edges to consider: $(a,b)$, $(s,b)$, $(p,d)$, $(s,d)$, $(p,c)$, $(s,c)$
  - Node $p$ is a Steiner node
Second Iteration (cont)

- Case (e) results in minimum delay: $t(c) = 268.6\, ps$
  - Add $(p, c)$

\[
t(c) = 268.6\, ps
\]
Third Iteration

- 7 edges to consider

![Graphs](image)
Fourth Iteration

- 6 edges to consider

\[ t(b) = 606.3\text{ps} \]
\[ t(d) = 557.3\text{ps} \]
Final SERT Result

- Maximum Elmore delay is $t(b) = 606.3\, ps$
  - Two Steiner nodes used
ERT vs SERT

- Not a fair comparison
  - Technology parameters are different (65nm vs 1.8μm)

\[ t(b) = 4630\text{ps} \quad \text{and} \quad t(b) = 606.3\text{ps} \]