Advanced Digital Design with the Verilog HDL

Errata and Revisions

Rev 04/13/2004

The revisions posted in this file will appear in the second/revised printing of the text available September 2003.

Notation: LT = lines from the top of the page, LB = lines from the bottom of the page.

Chapter 2
p. 19: In Fig. 2-8, the label b’ in the top right Venn diagram should be a’.

Chapter 3
p. 72: Change S’ and R’ to S and R in Figure 3-2.
p. 79: The inputs labeled OE in Figure 3-13 should have a bubble.
p. 88: The cells of the Karnaugh maps in Figure 3-21 should contain "x" when q2q1q0Bin = 0101
p. 89: Add a reset line to the flip-flops in Figure 3-22.
p. 94: Add a reset line to the top flip-flop in Figure 3-29.

Chapter 4
p. 104, 2LT: Change a1 to a.
p. 105, 5LT: Remove bold from ).  7LT: Remove bold from ).
p. 109, Fig. 4-6a Change label to Add_full_0_delay.
p. 111, 16LB: Change w2, c_in to c_in, w1.
p. 112: Change Add_half_0_delay to Add_full_0_delay at the left block in Figure 4-7c.
p. 138, 2LB: Change "value of 0" to "value of 0 (j = 0, k = 1) ... value of 1 (j = 1, k = 0)"
p. 140: 1LB, delete "encoded"
p. 141, 7LT: Change "continuous assignment statements" to "gate-level models"
p. 141, 9LT: Change (1,2,4,4) to (1,2,4,5)

Chapter 5
p. 126, 9LT: Change $stop to $finish.
p. 145, 10LB: Change the reference to Figure 4.7 to Figure 4.5.
p. 149: Modify AOI_5_CA3 to include x_in5.
p. 152: In Latch_Rbar_CA change reset to reset_bar
p. 159, 6LB: Delete B, C, D, from the port of the model for shift_reg_P.
p. 160, 1 LT: Change reset to rst.
p. 175, 6LB: Change Tap_Coefficient to 8'b1111_0011 to match results in Fig 5-16.
p. 177, 8LT: Change Tap_Coefficient to 8'b1111_0011 to match results in Fig 5-16.
p. 181,16LB: Change Tap_Coefficient to 8'b1111_0011 to match results in Fig 5-16.
p. 184: In caption for Figure 5-19, change waveforms to waveform
p. 184, 4LB: Replace <= with < (endless loop!)
p. 185: In add_4_cycle, some compilers require re-declaration of the array size [5: 0] for sum
p. 188: 2LT, some compilers require re-declaration of array size with reg.
p. 188: 8, 9LT: Interchange line 8 with line 9 to conform to the arguments in the call of the task.
p. 190, 4LT: Delete comma at the end of the list of ports
p. 191: The floating input to the 3-input or-nand gate should be connected to operand_2[1], as shown below.
p. 197, 2LB: Change "as a synchronous entry" to "as an asynchronous entry"
p. 199, 2LT: Change reset_== 0 to reset_ => 1
p. 215 Change the caption of Figure 5-39 to read "A situation requiring synchronization across clock domains."

p. 221, 15LT:- Some compilers require re-declaration of array size [3: 0].

p. 222, 9LT: Change the comment to be // Assert all columns

p. 222, 1LB: Some compilers require re-declaration of array size [3: 0] with reg

p. 223, 9LB: Move the comment for the "one-hot" codes to the line "always @ (Key) begin"

p. 224: 4LB, Change #25 to #20

Chapter 6

p. 232 The description of the behavior of the arithmetic shift in problem 5.39 should say that a right shift loads the MSB back into the MSB.

p. 250 Replace Figure 6-16 with the the figure below.

p. 254 Figure 6-18b incorrectly duplicates Figure 6-22c. The correct figure is shown below.
p. 270, 5LT: Change bus_enabled to bus_enable
p. 271, 7LT: Change value of conditional assignment from data_to_from_bus to 32'bza
and change reg_to_bus to ckt_to_bus.
p. 272, 14LB: delete "swap"; 16LB: insert comma after data_b and delete comma after clk.
p. 287, 288: Modify the event control expression of the level-sensitive behaviors for the next
state to include or En
p. 288: The comment in Seq_Rec_3_1s (Mealy and Moore) should state that the encoding is
binary.
p. 322, 9LT: temp = temp >> 1;
p. 339, 6LB: Change 5.45 to 5.46.
p. 341: Problem 11 should state that the model in Example 6.26 uses a binary opcode. The task
in Problem 11 is to design with a one-hot code.
p. 362: The caption for Fig. 7-12 has the labels for (d) and (e) in reverse order.

Chapter 7
p. 367, 22LT: Change M2_MEM to M2_SRAM.
p. 368, 369, 370 Some compilers may require re-declaration of array size with reg.
p. 377: 19LB: Place // before Flush Memory
p. 379: Delete Data Bit 7 in Figure 7-15.
p. 390: Delete Data Bit 7 in Figure 7-24.
p. 391: Edit Figure 7-25 to change repeated outputs to inc_Bit_counter and clr_Bit_counter.
p. 406: Change all assignments to <= in ring2_count.
p. 410: The data shown in Figure P7-15c includes an extra pattern for Data = aaaaH that is not
included in the testbench given on p. 412.
p. 411, 2LT: Expand the sensitivity list to include tmp and Gap. Their omission does not affect
the simulation, but the model will draw a warning by a synthesis tool.
p. 412, 21 LT: Change the expected Gap to 1

Chapter 8
p. 475, 2LB: Change form to from
p. 490: The flip-flops in Figure 8-61 have the labels for Q and D reversed
p. 535, 9LB: Change fork to begin
p. 535, 6LB: Change `join` to `end`

**Chapter 9**
p. 585: In Figure 9-16, change the third row from the bottom to be 4 7 5 6
p. 589, 1LT Delete `end` at end of line; 2LB insert `end` at end of line.
p. 606, 3LT: change 9-25 to 9-29.

p. 627, 2LT: Interchange `buff_size` and `word_size`. 3LT, 4LT, 11LT: Interchange with 12LT
16LB, 17LB: Change `wire` to `assign` to satisfy some compiler's requirement for redundant array
declarations. 18LB: Interchange `buff_size` and `word_size`. 

p. 636, 6LT: Change Dual_Port to Buffer.

p. 683: In Figure 10-27, place a conditional output asserting `Add` on the edge to `S_done` from the
decision diamond testing \( m = 1 \). Annotate the edge with the register operation `product <=
product + multiplicand`.

**Chapter 10**
p. 671(Fig 10-19), p. 677 (Fig 10-22), p. 714 (Fig 10-50) change `Load_word` to `Load_words`
p. 693, 9LB Change leftmost to rightmost.

p. 694, Figure 10-35: In the third row from the bottom the empty cell should contain a 0.

p. 703, 18LT: `L_word = 4;`

p. 718, 6LB, 5LB: Replace code for expected value:

\[
(\text{All}_\text{Zeros}, \neg \text{word}2[\text{L}_\text{word} -1:0]) + 1) * (\text{All}_\text{Zeros}, \neg \text{word}1[\text{L}_\text{word} -1:0])+1)
\]

p. 719, 4LT Boldface `end`

**Appendix A**
p. 883, 6LT: Change `rtranif0` to `rtranif0`

**Appendix D**
p. 906: Interchange the text labels for multiplication and division in Table D-2.

p. 907: Replace Table D-3 with the table given below.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Operator</th>
</tr>
</thead>
<tbody>
<tr>
<td>~</td>
<td>Bitwise negation</td>
</tr>
<tr>
<td>&amp;</td>
<td>Bitwise and</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>^</td>
<td>Bitwise exclusive or</td>
</tr>
<tr>
<td><del>^, ^</del></td>
<td>Bitwise exclusive nor</td>
</tr>
</tbody>
</table>

**Appendix G**
p. 940, 6LT, 7 LT: Change `@` (posedge ...) to `always` @ (posedge ...) 

**Appendix I**
p. 946, 958, 959: Some compilers require re-declaration of array size with `reg` in Verilog 1995
p.947: Insert `reg q_out` in table for Verilog 1995

p. 951: Remove the `begin/end` keywords in Figure I-10.

p. 952: Size `a_byte` to [7: 0] and `b_byte` to [3: 0] in Figure I-11.

p. 954: In Table I-16, insert semicolon 64'sd2;

p. 955: In Table I-18, insert semicolon diff / v;

p. 955, 8LT Change `pass` to `passed`.

p. 958, 6LT: referenced

p. 958 In Figure I-24 declare `reg c_out` and `reg sum`

p. 959: In Figure I-25 declare `reg diff`;

p. 993, 5LB: Insert comma clear, clock