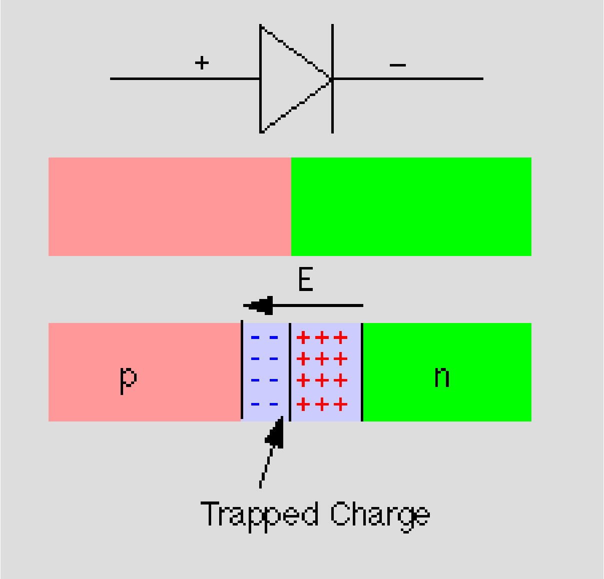
ECE 3060
VLSI and Advanced Digital Design

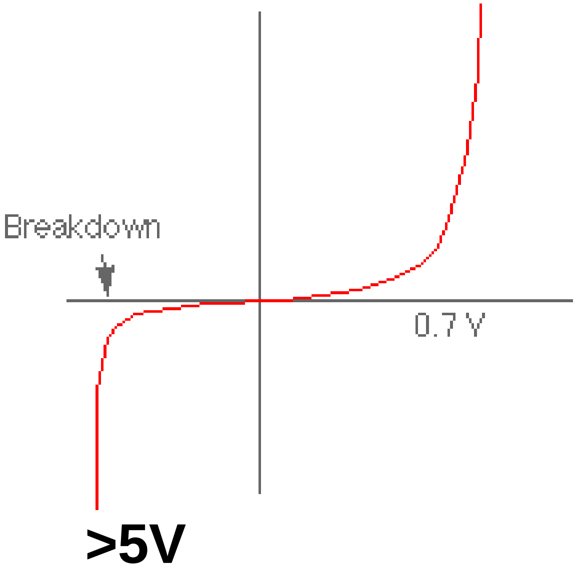
Lecture 2

MOS Transistor

The pn Junction

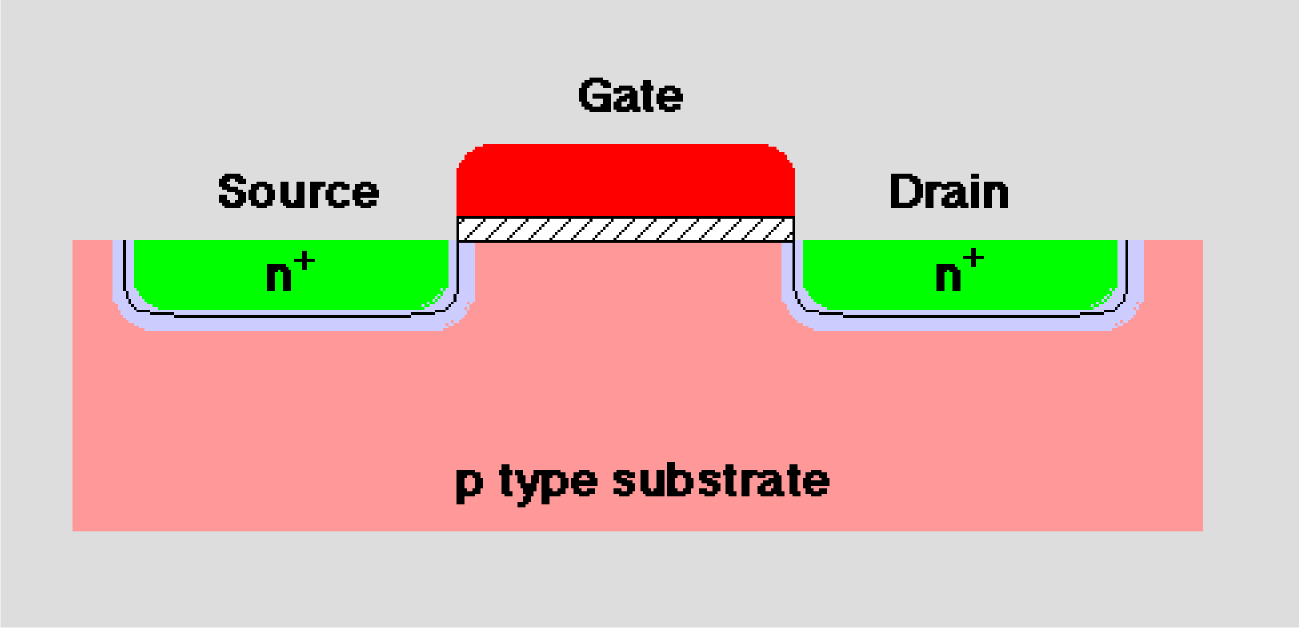
- **Majority carriers diffuse from n to p and from p to n, leaving trapped impurity (donor) ions behind**
- **Width of depletion region is inversely proportional to carrier concentration**





MOS Subthreshold Region

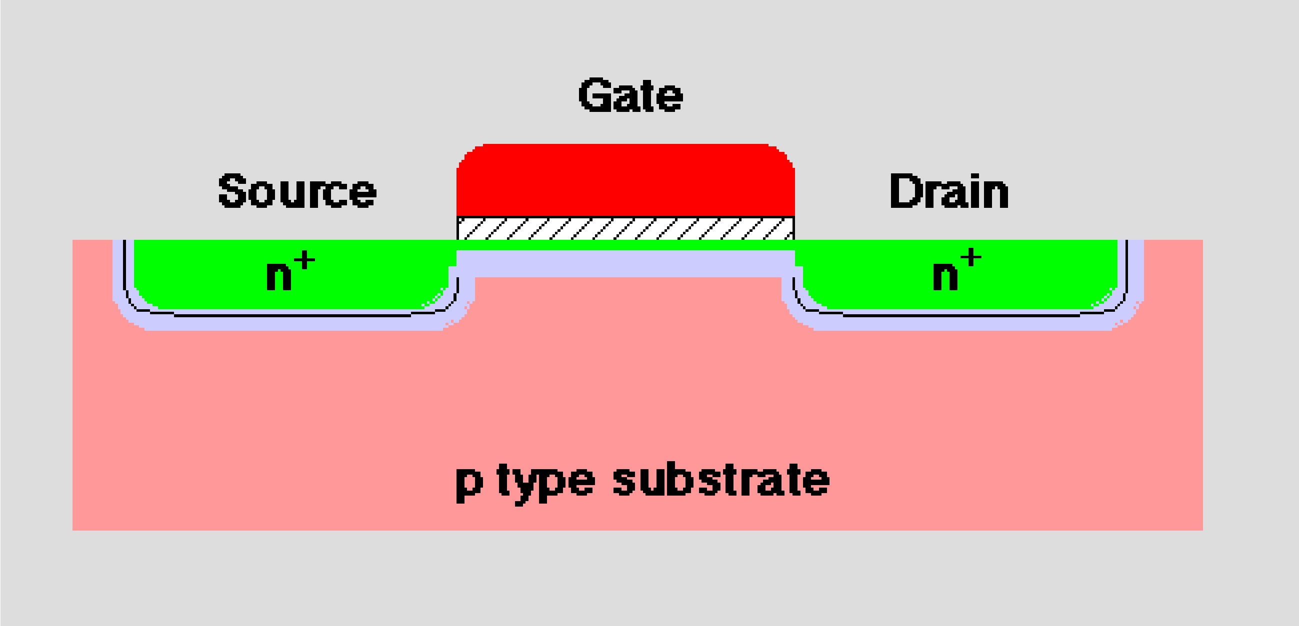
- **Subthreshold Region** $I_{ds} \approx 0$, $V_{gs} \leq V$



- **Subthreshold current is due to reverse bias leakage current of diode between diffusion and substrate**

MOS Linear Region

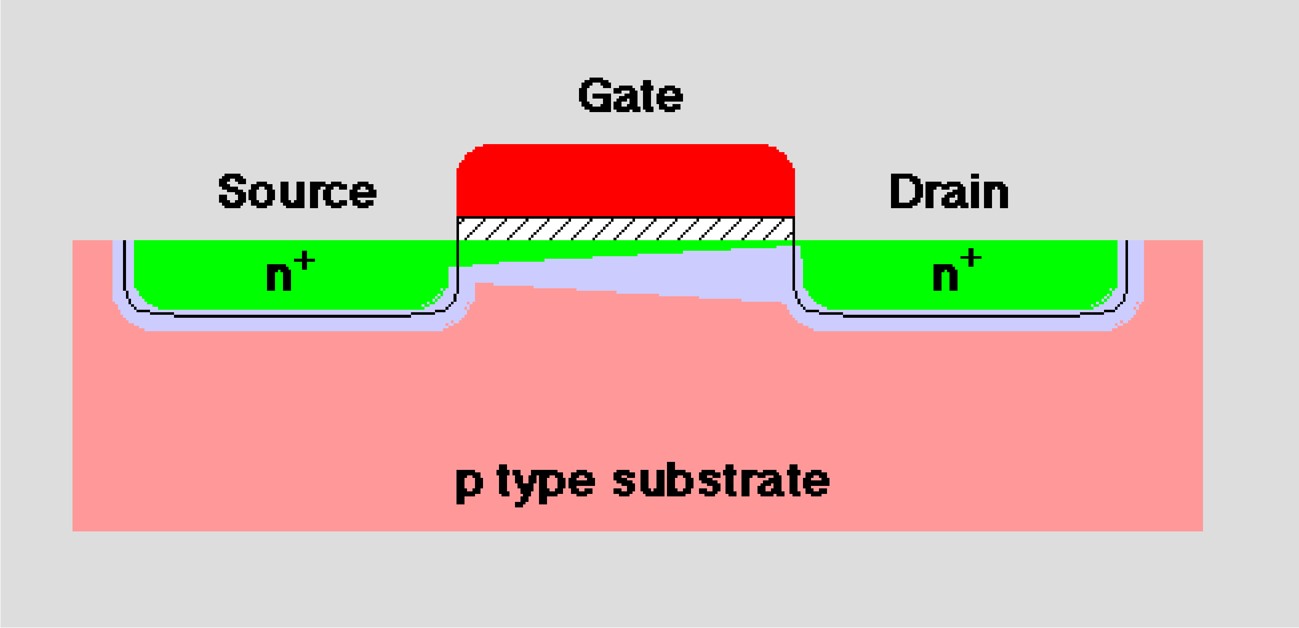
- **The inversion layer (channel) is symmetric, until:**



- $$I_{ds} = \beta\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad 0 \le V_{ds} \le V_{gs} - V_t$$

MOS Linear Region

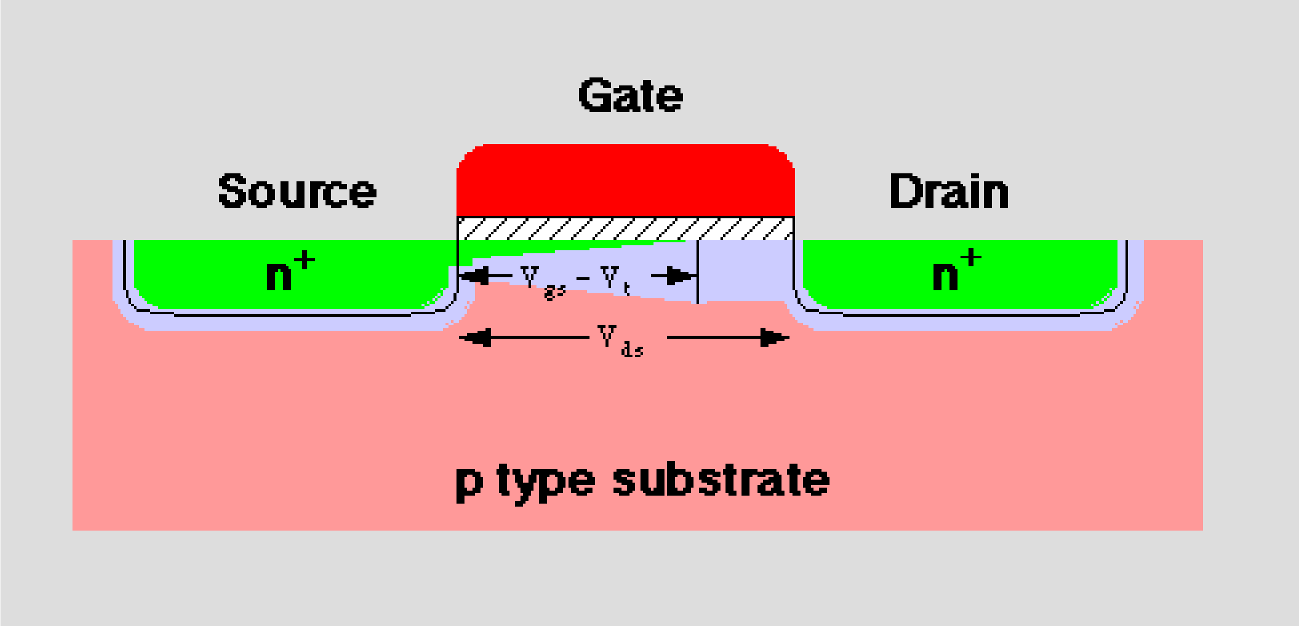
- **Transverse electric field distorts the channel**



- $I_{ds} = \beta\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad 0 \le V_{ds} \le V_{gs} - V_t$

MOS Saturation Region

- **Channel is pinched off when** $V_{gs} - V_t \leq V_{ds}$



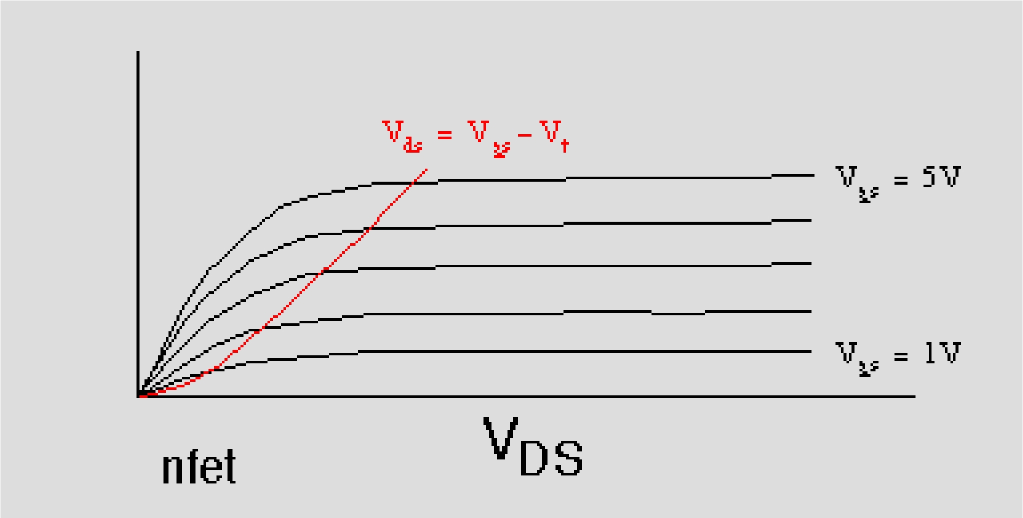
$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 \quad 0 \leq V_{gs} - V_t \leq V_{ds}$$

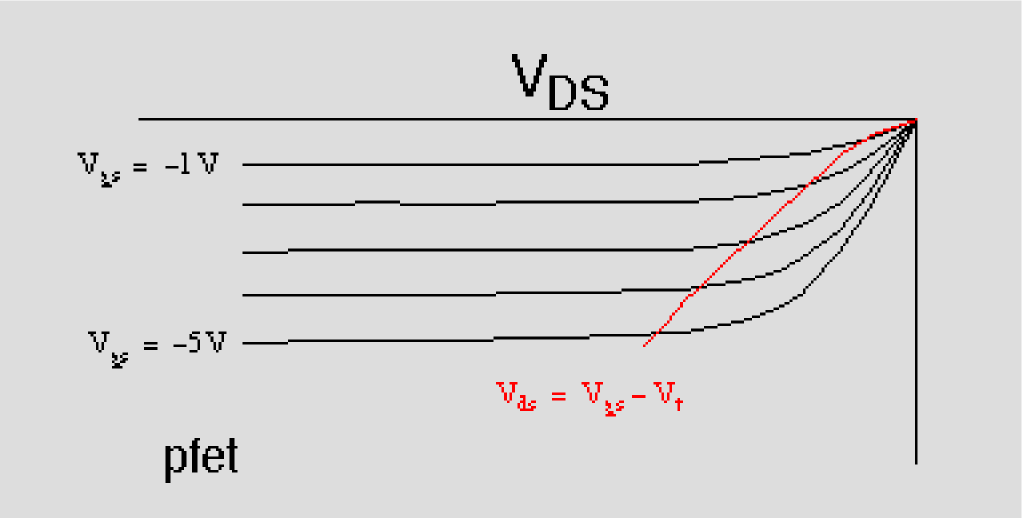
- **Current is swept through depletion region electric field after leaving channel.**

Channel Length Modulation

- When the device is in saturation the effective channel length is decreased
- Therefore the transconductance is increased
- λ is an empirical channel length modulation factor
- $I_{ds} = \frac{kW}{2L}(V_{gs} - V_t)^2(1 + \lambda V_{ds})$

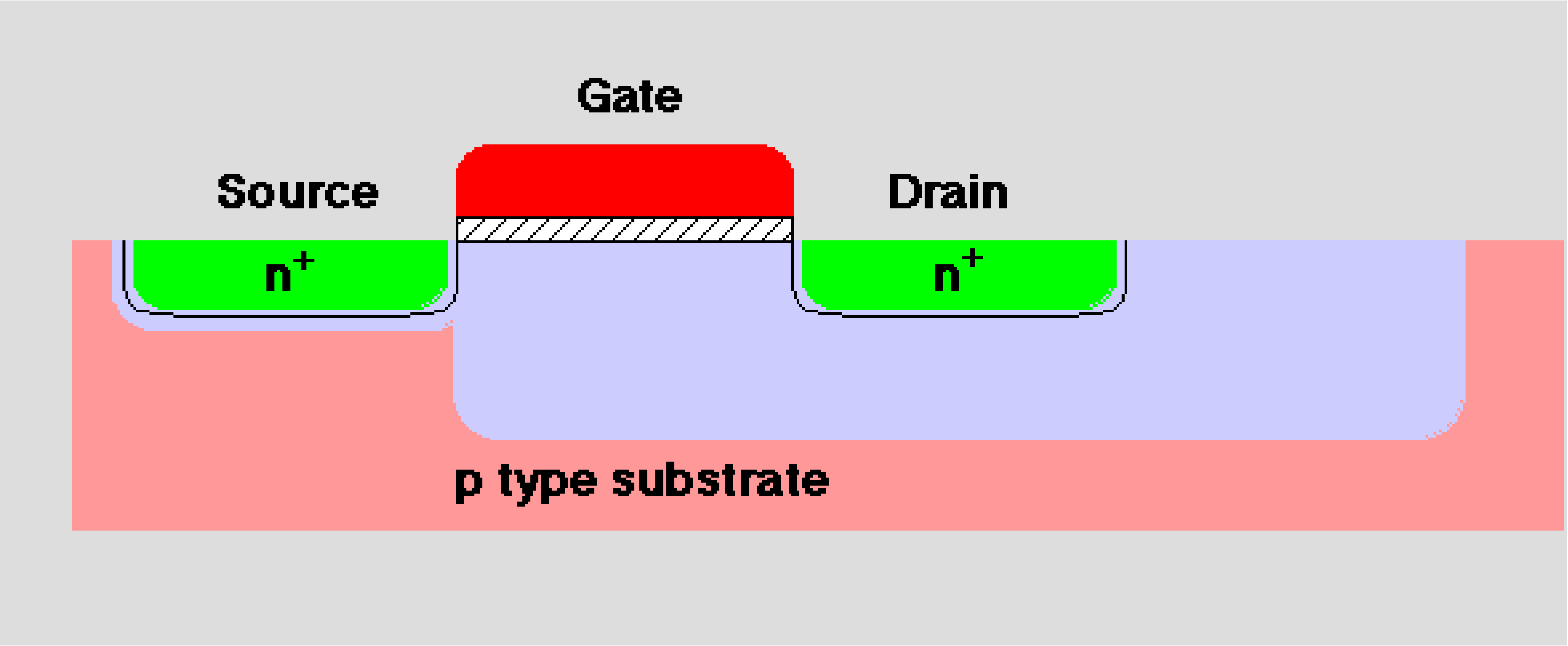
MOSFET Curves





Drain Punchthrough

- If drain voltage is sufficiently high, depletion region may extend all the way to the source
- Then carriers are diffused from source into depletion region, and swept through E field to drain.



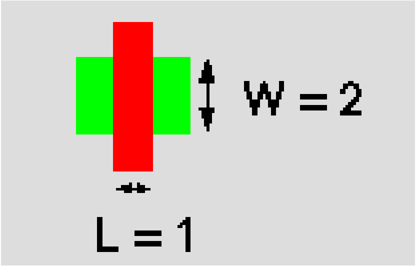
Hot Carriers

- **As we scale down gate length L, and if Vdd is fixed, the channel E field is increased.**
- **Since mean free path is fixed, charge carriers achieve higher velocity**
- **Hot electrons can ionize drain holes, which are repelled from the drain to the substrate**
  - **Substrate current**
  - **Latchup**
  - **Damage**
- **Lower Vdd**

Body Effect

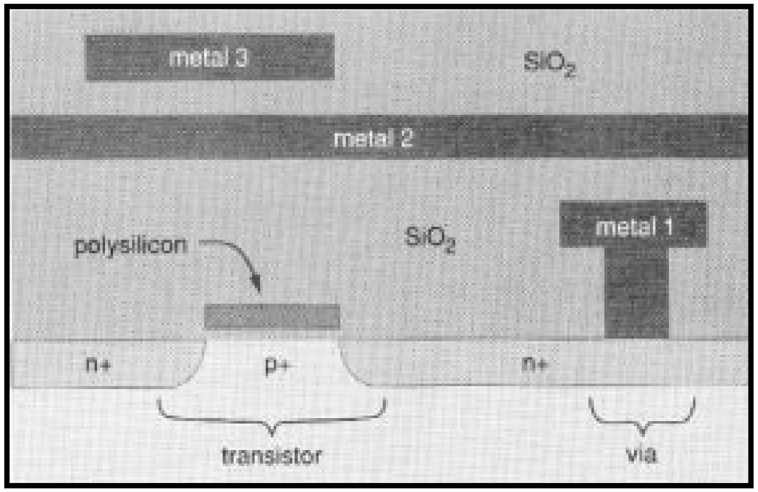
- When the source to substrate bias is positive, the channel substrate depletion region increases.
- This reduces the channel (charge neutrality), and hence increases the threshold voltage.
- Body effect may adversely impact the onset of switching, and hence gate delay, in complex gates with long chains of FETS.

Transistor Sizing



- **Process transconductance:** $k = \mu \frac{\varepsilon}{t_{ox}}$
- **Device transconductance:** $\beta = k \frac{W}{L}$
- **Carrier mobility depends on type** $\mu_n \approx 2\mu_p$

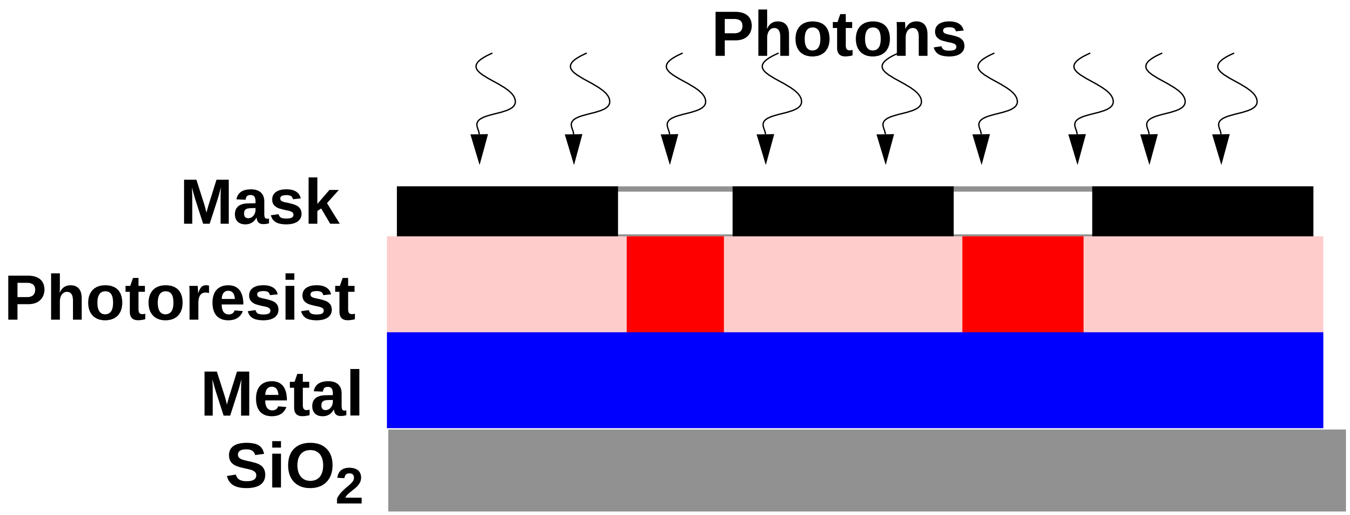
Structure of an IC



- IC is built on Si substrate with a number of processes
- Wires are fabricated from metal (Al or Cu) or polysilicon
- Insulation is silicon dioxide (SiO_2)
- Wires and contacts/vias are patterned by etching
- Transistor source/drain regions and wells are doped by diffusion
- Threshhold voltages are adjusted by doping channel by implant

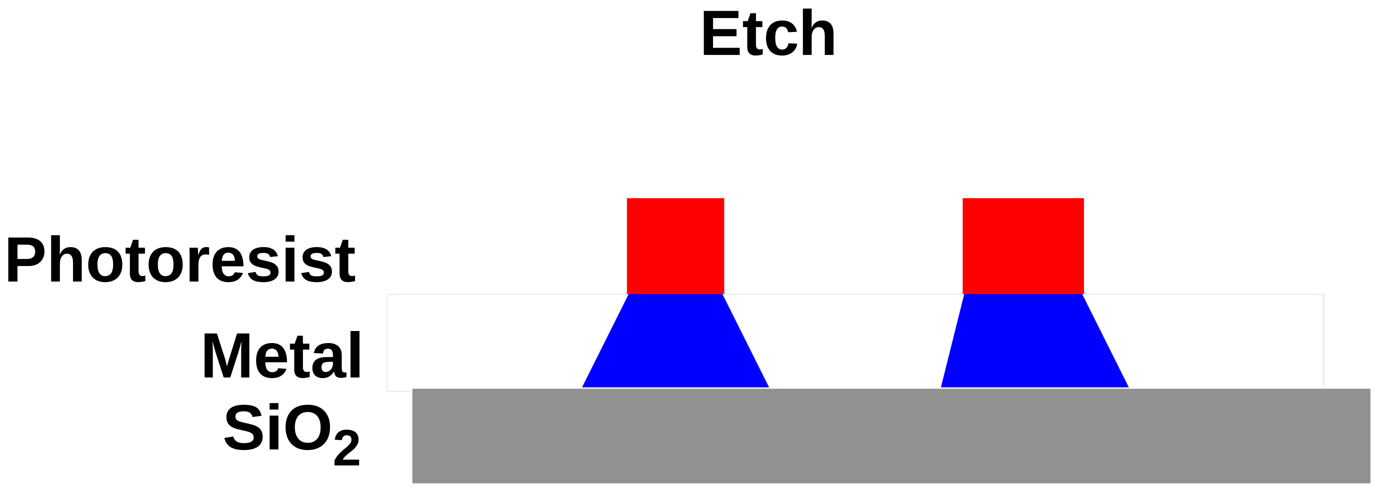
Photoresist

- An IC layer may be selectively etched or doped by applying, exposing and developing a photoresitive polymer layer.
- The polymer is hardened by exposure to actinic (high E) photons
- The unexposed photo resist is washed away leaving an etchant resistive mask



Etching

- A metal layer may be etched to form wires
- An SiO_2 layer may be etched to form contacts/vias
- The polymer may be used to control doping
- Finally the polymer is removed



Silicon Dioxide

- SiO_2 comes in three flavors
  - field or thick oxide is grown between transistors
  - thinox is a very thin layer used underneath the gate
  - SiO_2 is also deposited between layers as an insulator

Contact Fabrication