ECE 6133 Physical Design Automation of VLSI Systems
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Polish Expression Based Floorplanning

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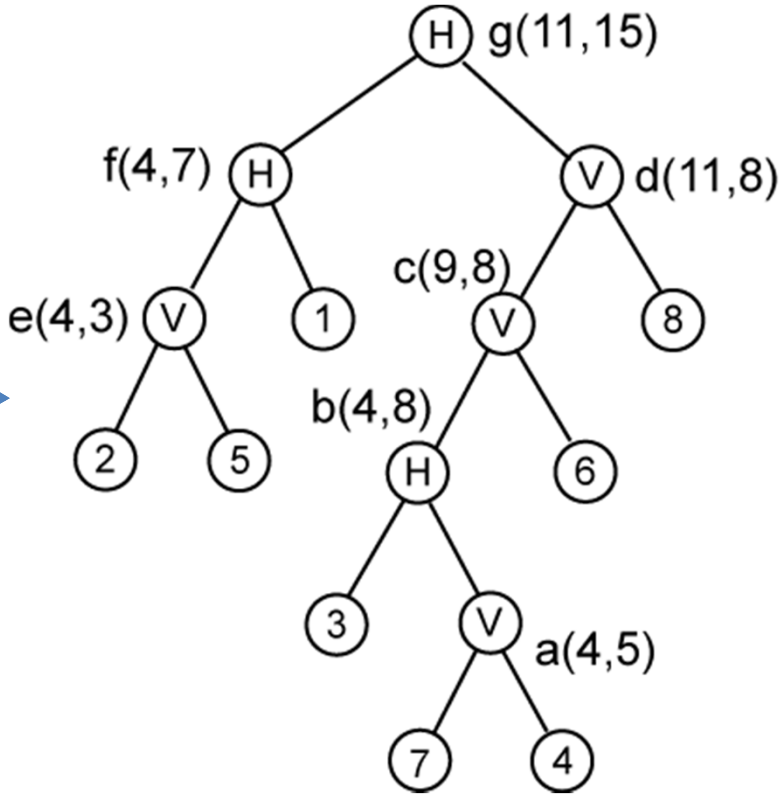
Project Overview

- What is the project about?
  - Using Normalized polish expression based Simulated annealing to determine the location of block in a floorplan.
- Goal of the project ?
  - Generate floorplan without overlaps and reduce the total floorplan area.
- Scope?
  - Used rectangular shaped hard blocks with no rotation allowed.
- Language used ?
  - C++ and Java

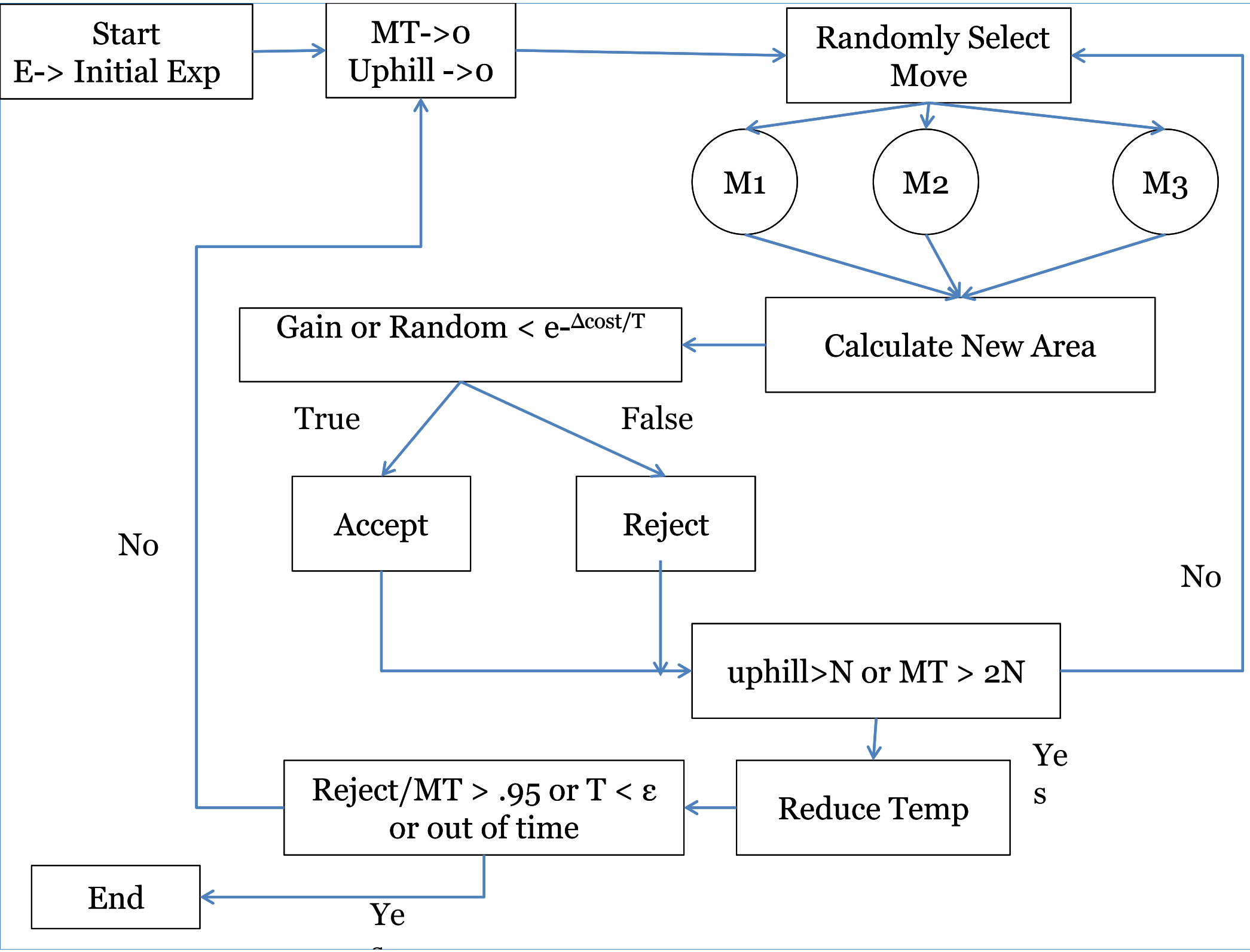
Normalized Polish Expression

- Polish expression can be obtained from the post- order traversal on binary tree.
- A polish expression which does not have any consecutive operators of same type (H or V).
- Using LIFO structure to convert polish expression to binary tree.

PE =25V1H374VH6V8VH



Algorithm


Start
E-> Initial Exp
MT->0
Uphill ->0
Randomly Select Move
M1
M2
M3
Calculate New Area
Gain or Random < e-Δcost/T
True
False
Accept
Reject
No
No
uphill>N or MT > 2N
Ye
s
Reduce Temp
Reject/MT > .95 or T < ε
or out of time
End
Ye

Data Structures

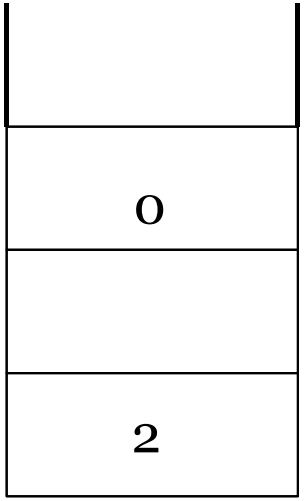
- Arrays
  - For storing width and height of each block.
  - For storing the polish expression.
- Stacks
  - For calculating area and generating trees.
- Binary Trees
  - For calculating the coordinates and generating graphs.

Implementation

- Parse the initial normalized polish expression and the size of the blocks from a text file.
- Store the polish expression as integer array where H and V are replaced by -1 and -2 respectively.
- Cost function was defined as the total Area of floorplan which is calculated as following :-

2	1	0	H	V

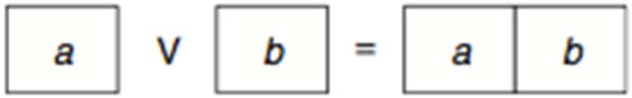
Block No	Size
0	1,3
1	5,1
2	3,3

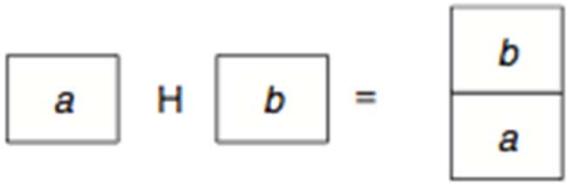


Width of H = 5 +
Area = 8*4 = 32

Calculating the floorplan coordinates

- Block Orientation :-

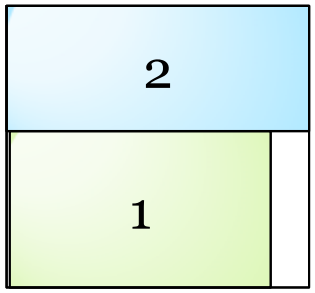




- First we create a binary tree from the polish expression by using a stack.
- While creating tree we also calculate the size of each room which is as following :-

H

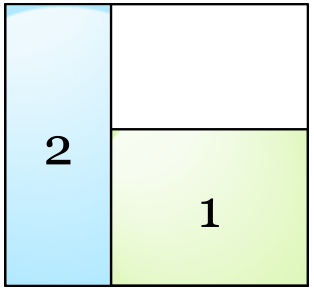
Height H
= Height 1 + Height 2



Width H
= Max(Width1 , Width2)

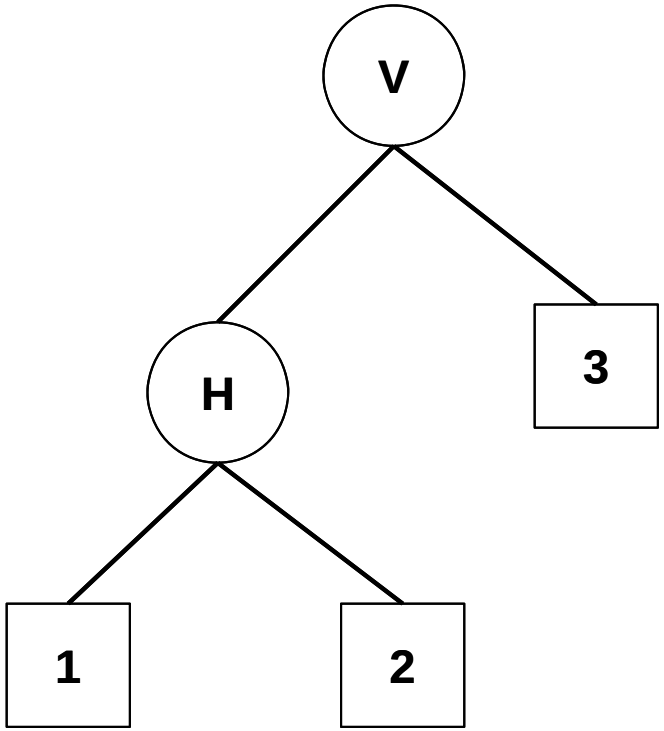
V

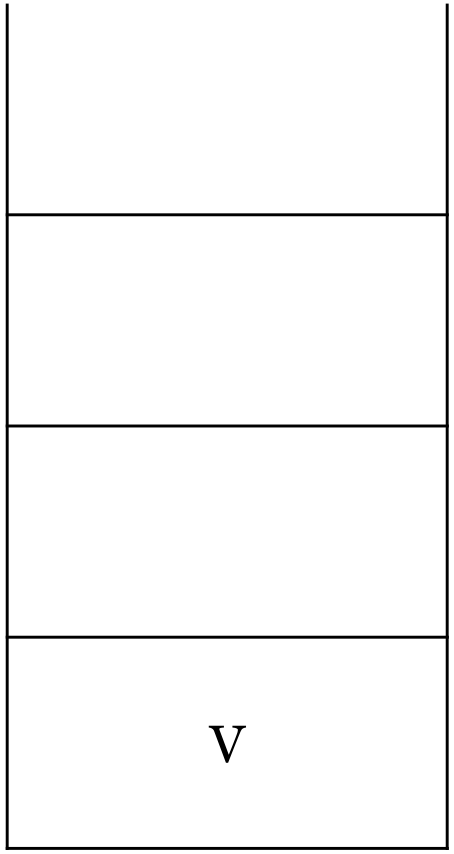
Height V
= Max(Height 1, Height 2)



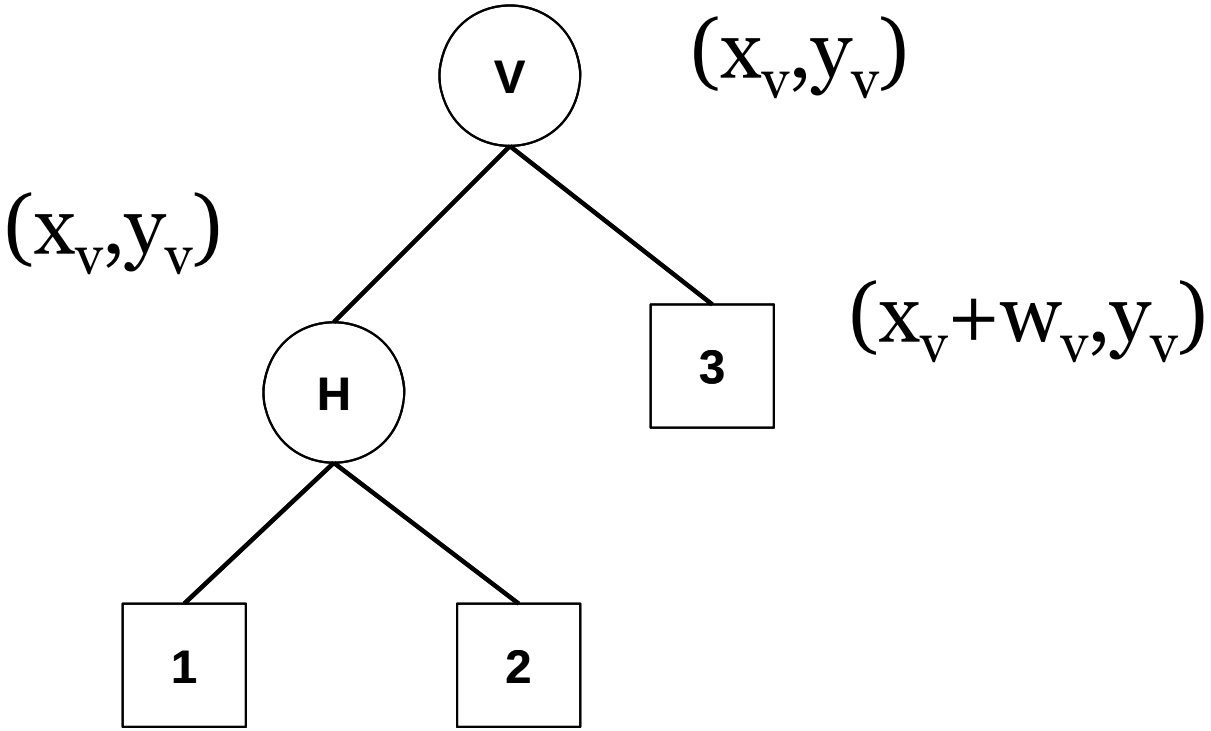
Width V
= Width1 + Width2

Initia
l

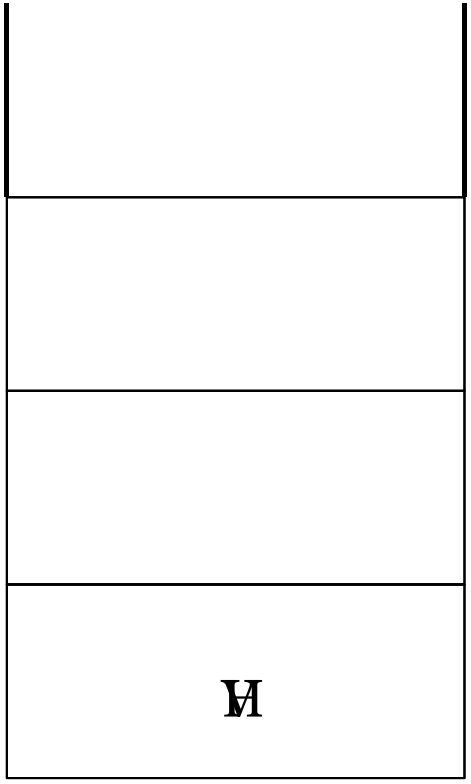




Push V in stack



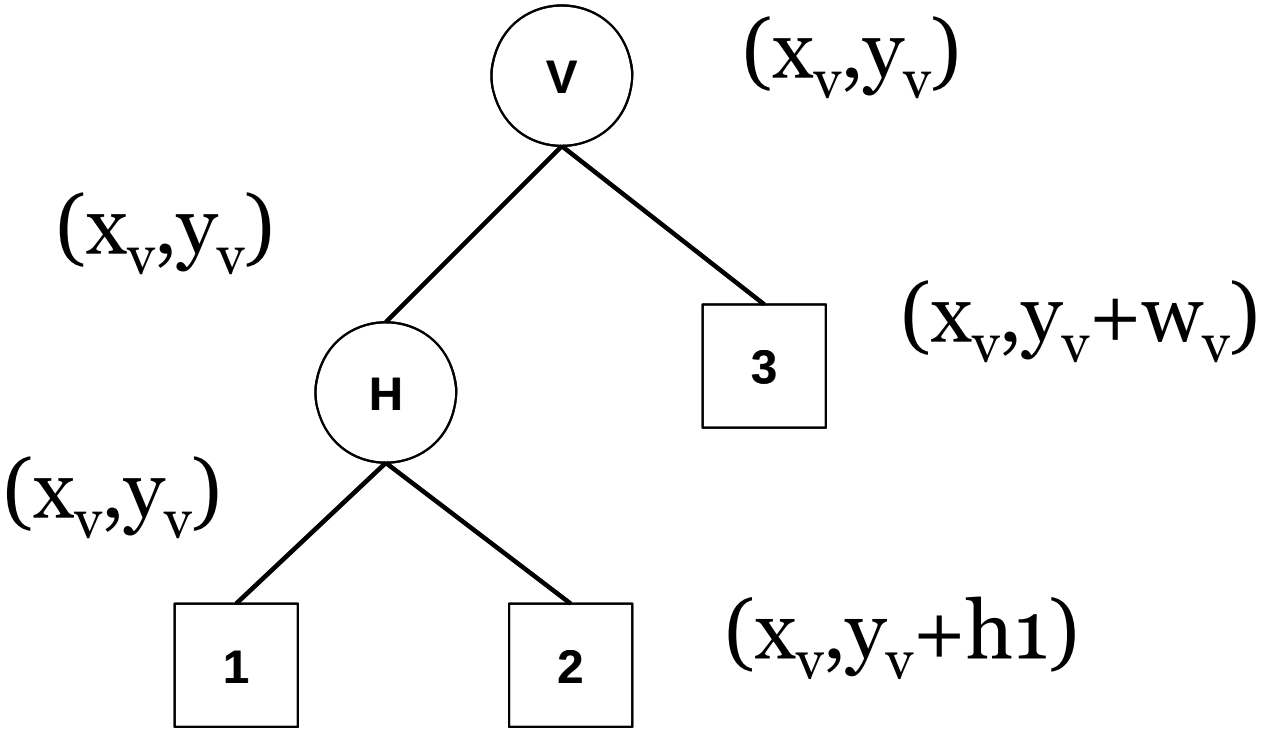
Pop V



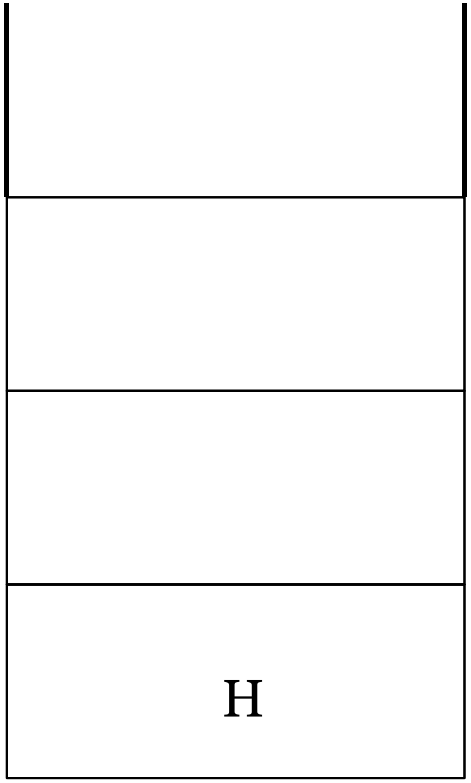
H's Coordinates = V's coordinates

X Cordinate of 3 = X coordinate of V + width of H.

Push H



Pop H



1's Coordinates = H's coordinates

X Coordinate of 2 = X coordinate of H

Y Cordianate of 2 =

Y coordinate of H + height of H.

Demo

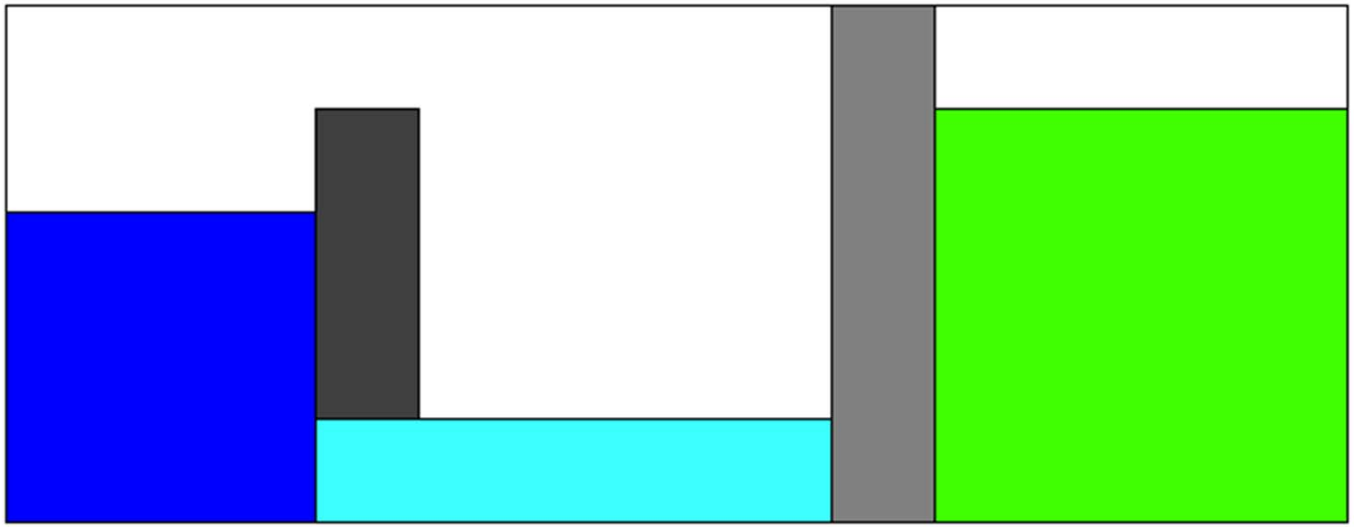
Parameters Used

No. of Block	Initial Temp	k	Cooling Ratio	Freezing Temp
5	200	16	0.96	144.277
10	320	16	0.96	2.38613
30	380	15	0.96	2.7201
100	3422	16	0.96	0.00393676
150	10040	20	0.99	0.000032

Floorplans

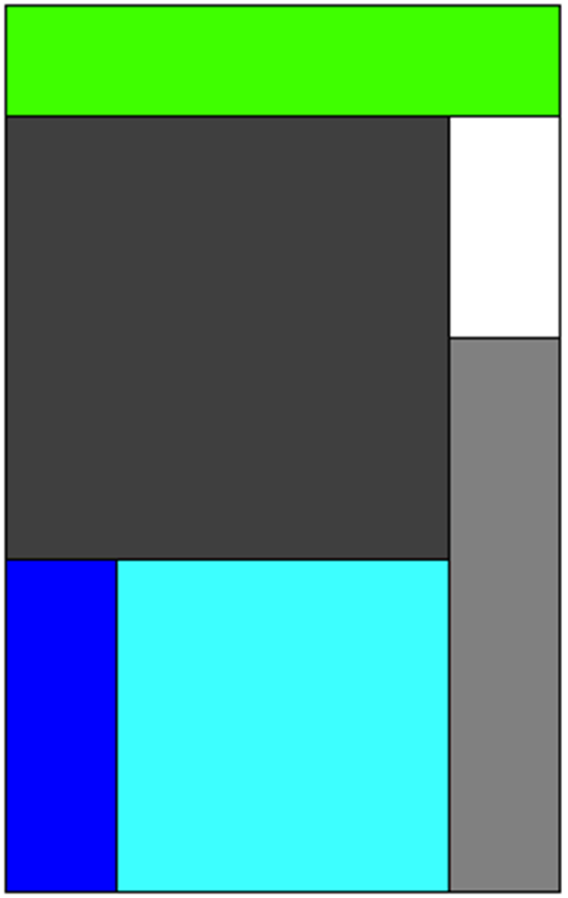
5 Blocks

Initial



Area = 65

Final

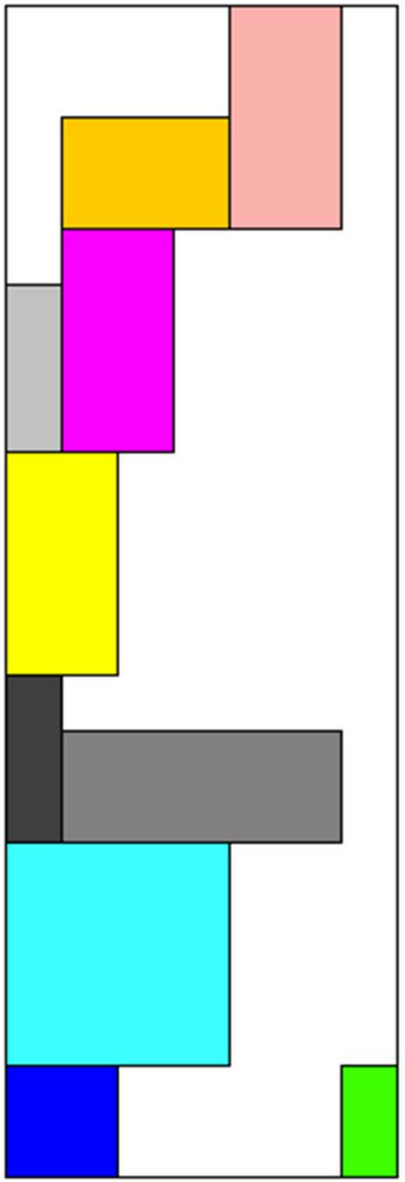


Area = 40

10 Blocks

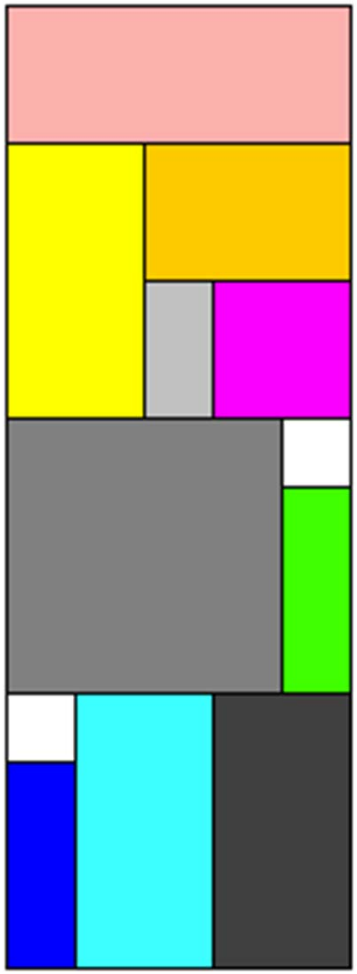
Initial

Area = 147



Final

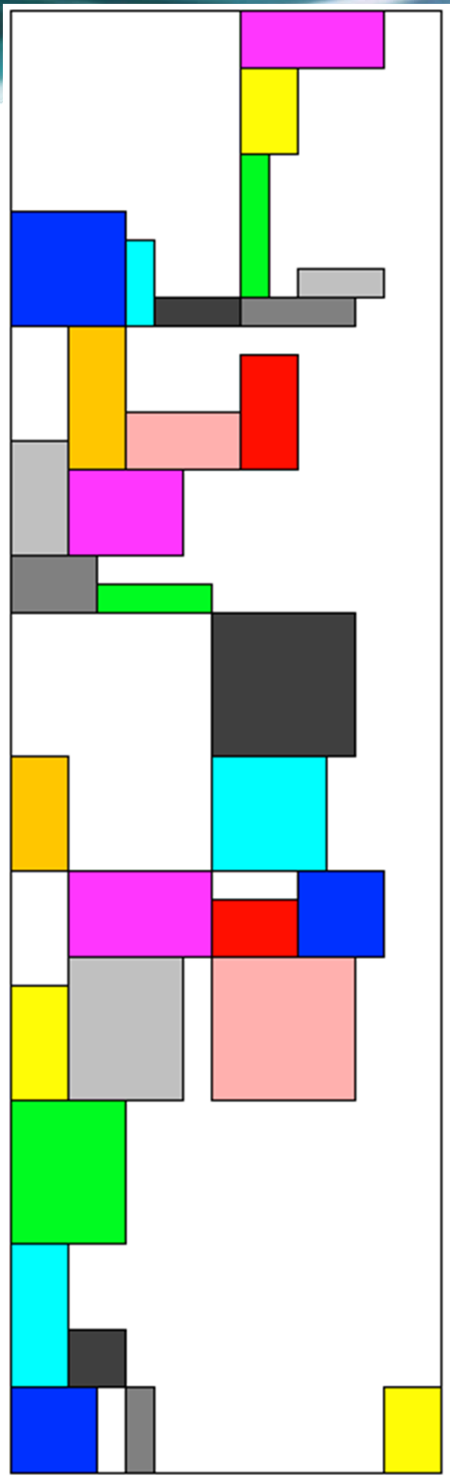
Area = 70



30 Blocks

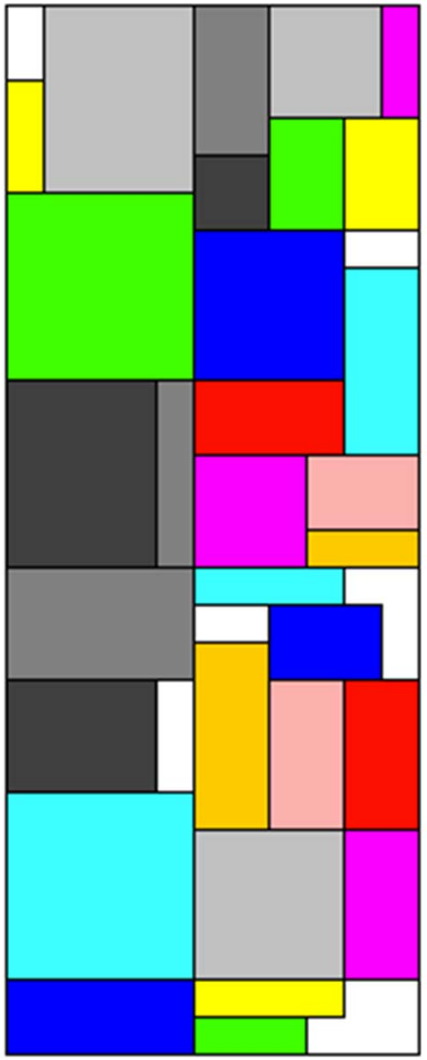
Initial

Area =1075



Final

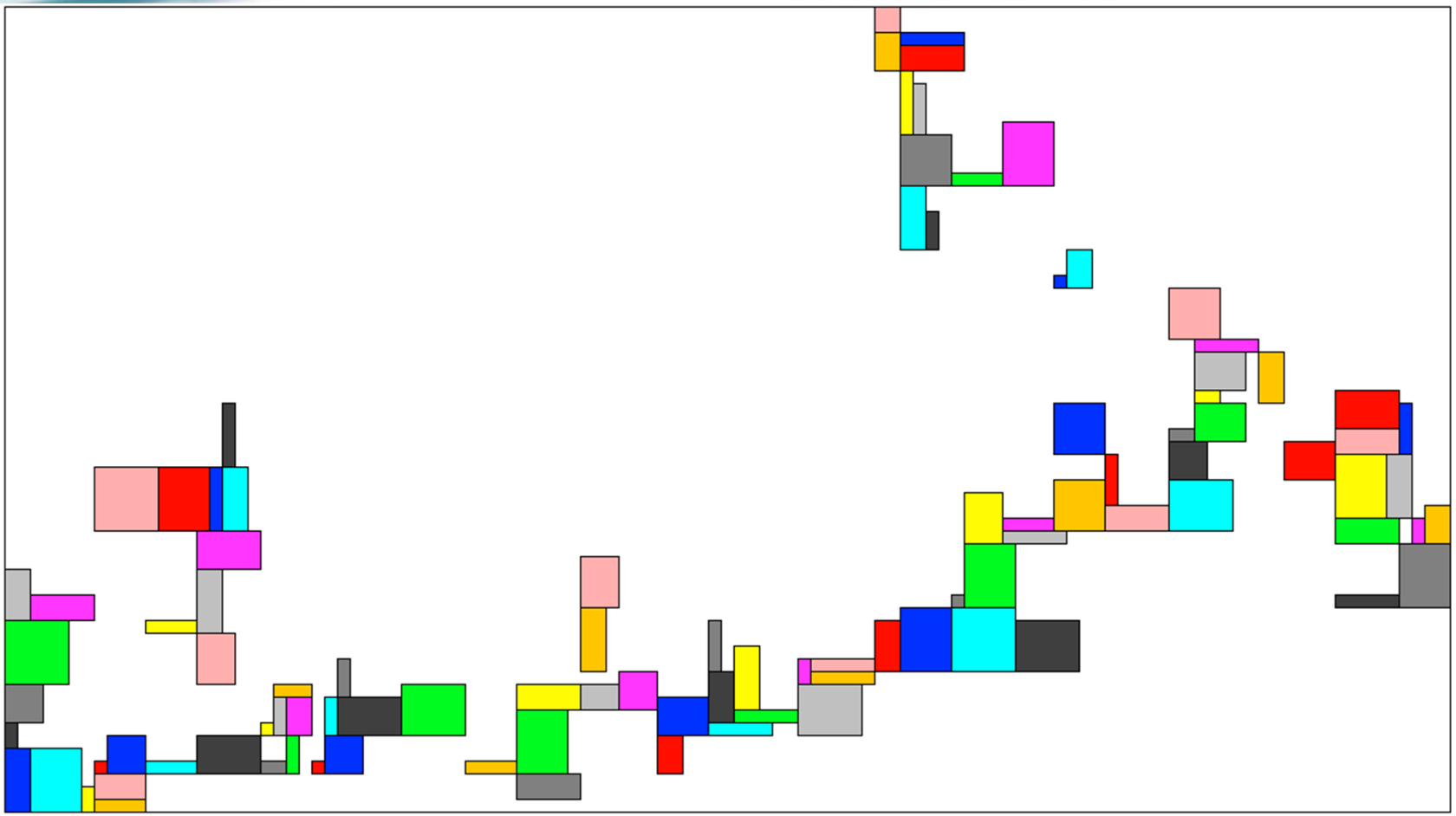
Area = 308



100 Blocks

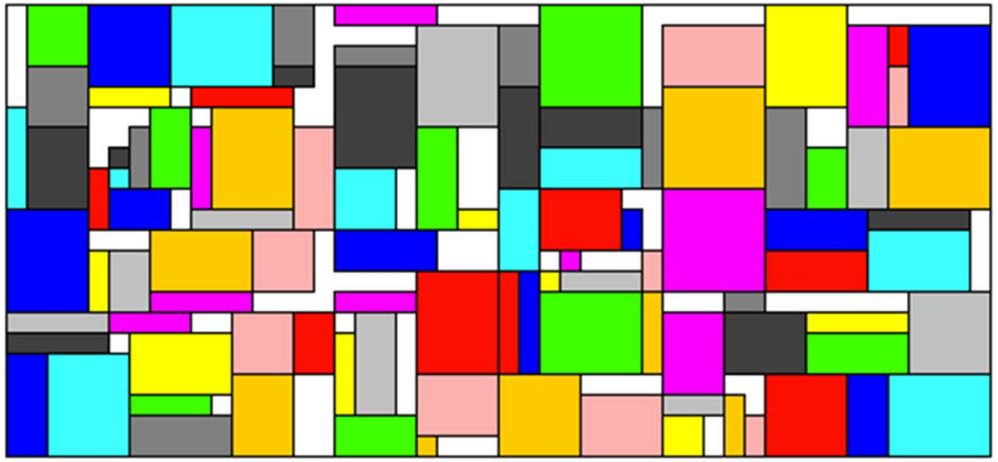
Initial

Area = 7119

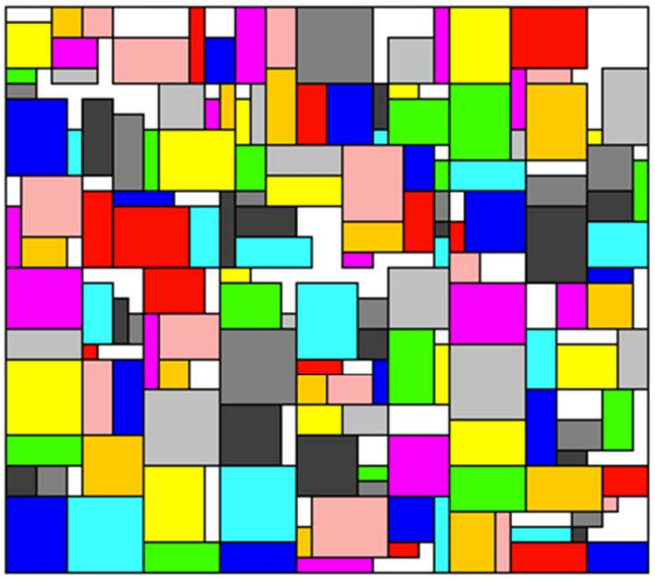


Final

Area = 1056

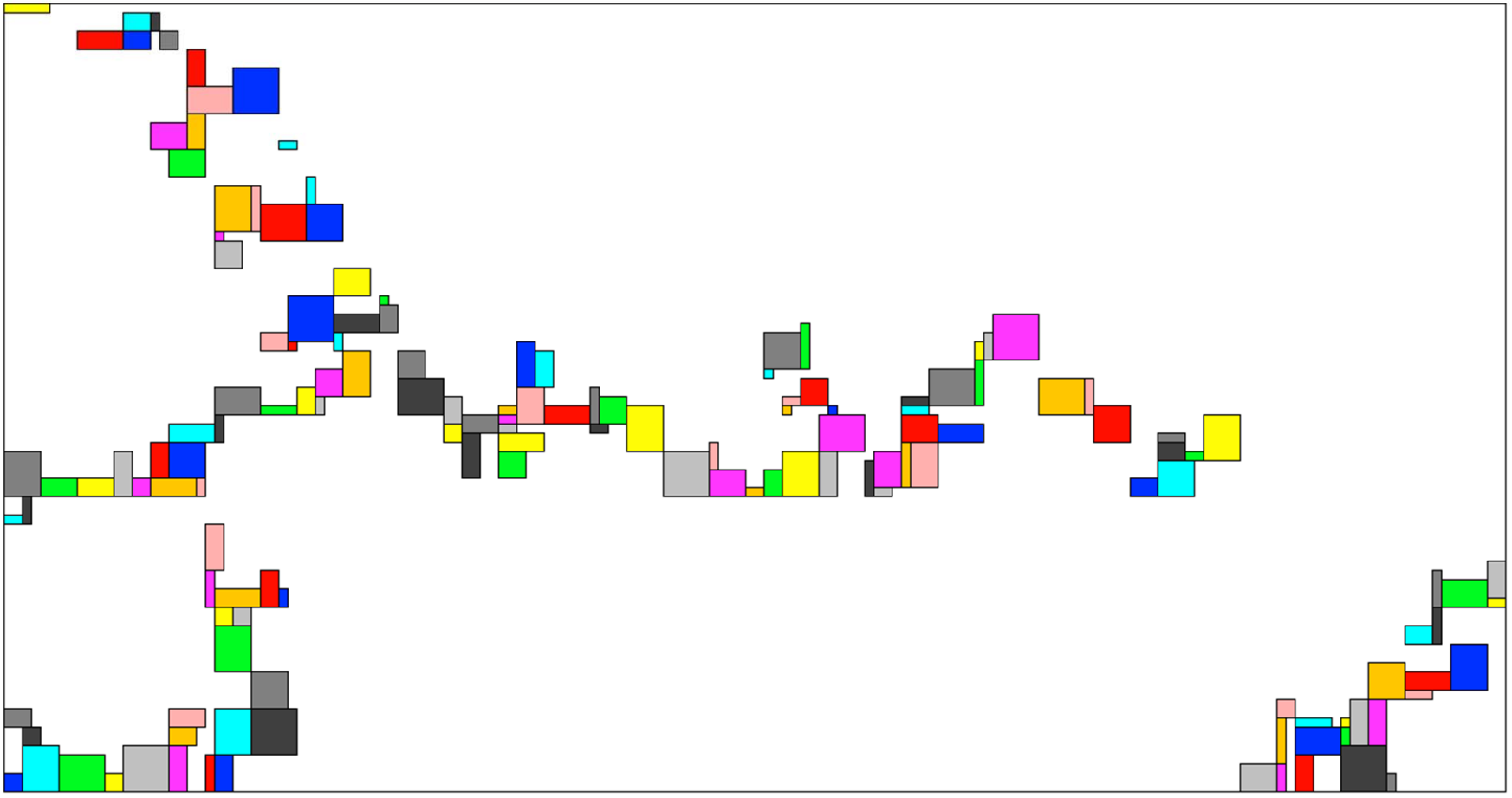


150 Blocks



Final

Area = 1554



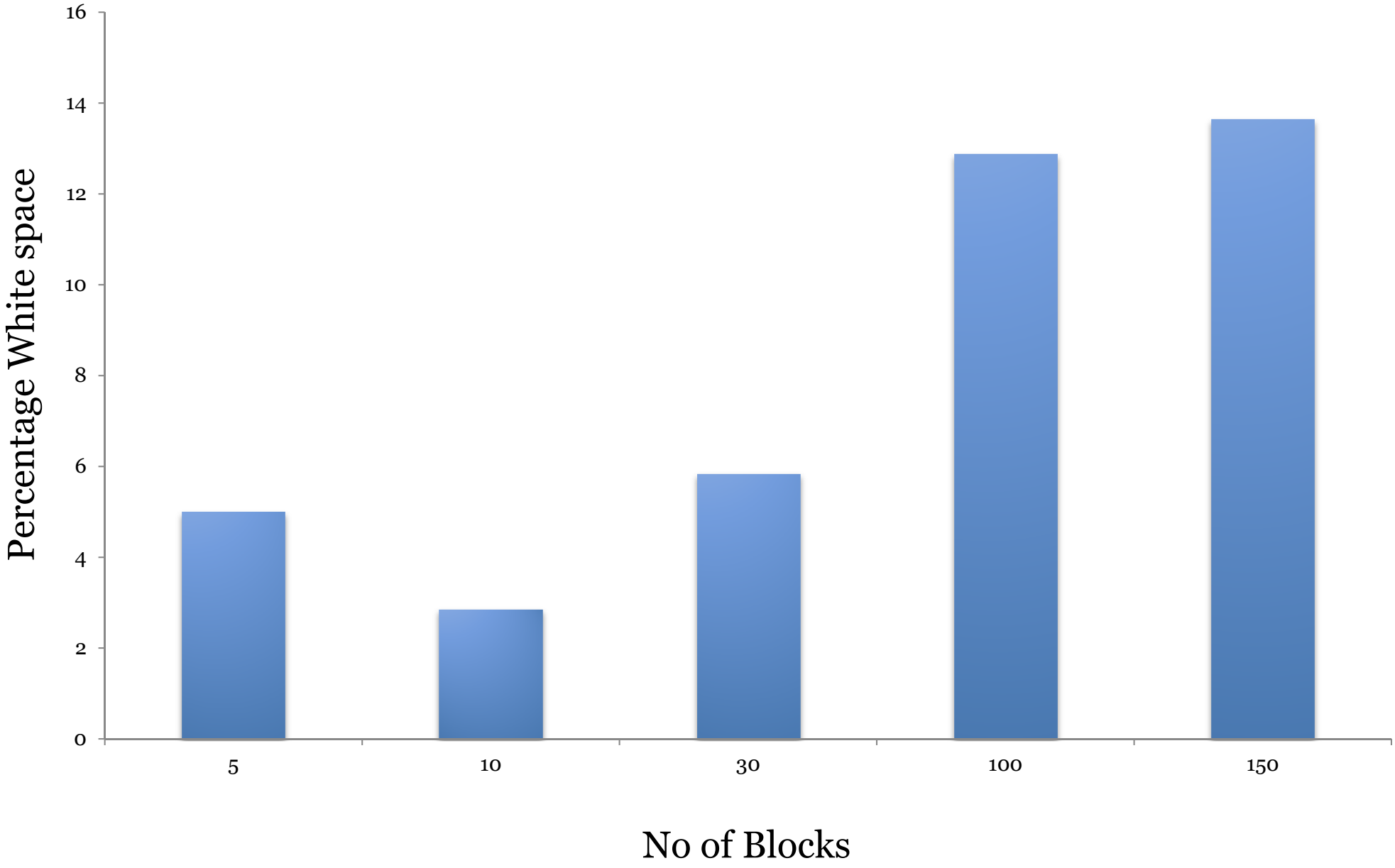
Initial

Area = 14104

Experimental Results

No. of Block	Initial Area	Final Area	Percentage Improvement	Time in Min
5	68	40	41.17647059	0.00006625
10	147	70	52.38095238	0.002007383
30	1075	308	71.34883721	0.017282667
100	7119	1056	85.16645596	0.527993333
150	14104	1554	88.98184912	8.006683333

Percentage White Space



Challenges

- Finding the initial parameters for simulated annealing which give minimum floorplan area.
- Reducing the run time and the memory requirement for simulated annealing.

Future Scope

- Use wire length as additional parameter in the cost function for simulated annealing.
- Add support for soft and L shaped blocks.

Conclusion

- Simulated annealing can reduce the floorplan area significantly but for the large circuits with higher initial temperature it has a long runtime.
- Runtime depends on the no of blocks, initial temperature, cooling ratio, no of moves per temperature and freezing temperature.
- No of rejected moves are more at higher temperatures.
- For our implementation there was good reduction in the floorplan area with low runtime.

Questions ?

Thank You

Reference

- Sung Kyu Lim, "Practical Problems in VLSI Physical Design Automation," Springer, July 2008
- D. F. Wong and C. L. Liu, "Floorplan design of VLSI circuits", Algorithmica, 4(1), pp 263-291, 1989.