Introduction

ECE6133
Physical Design Automation of VLSI Systems

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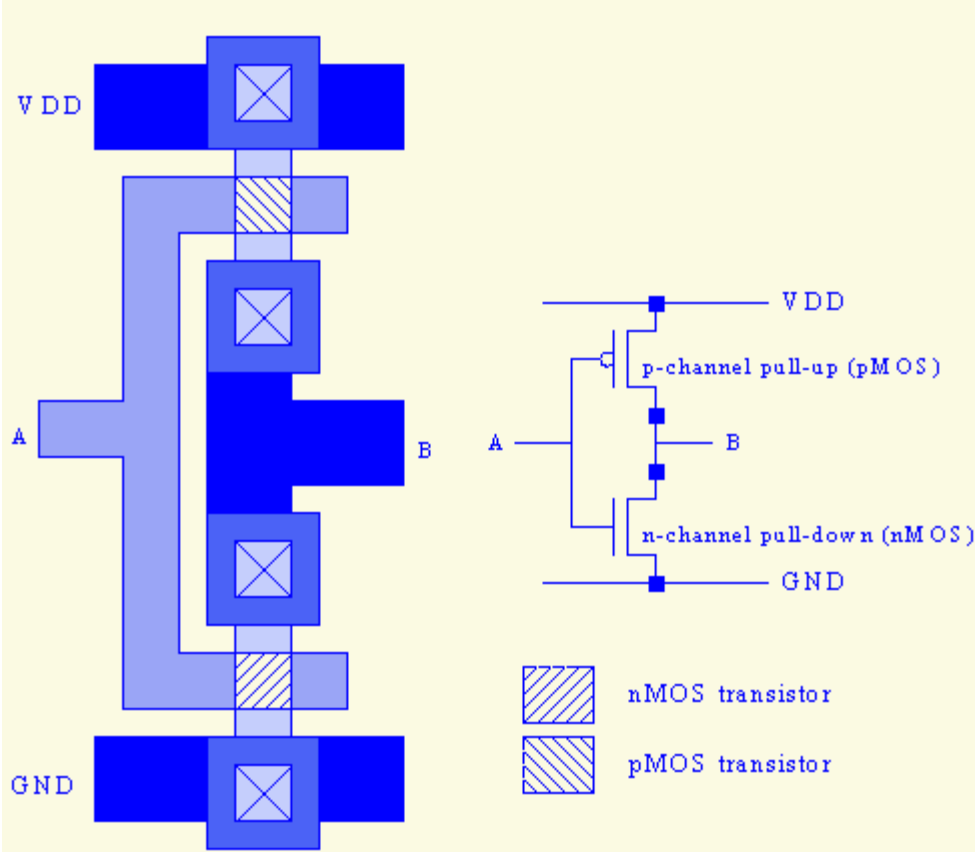
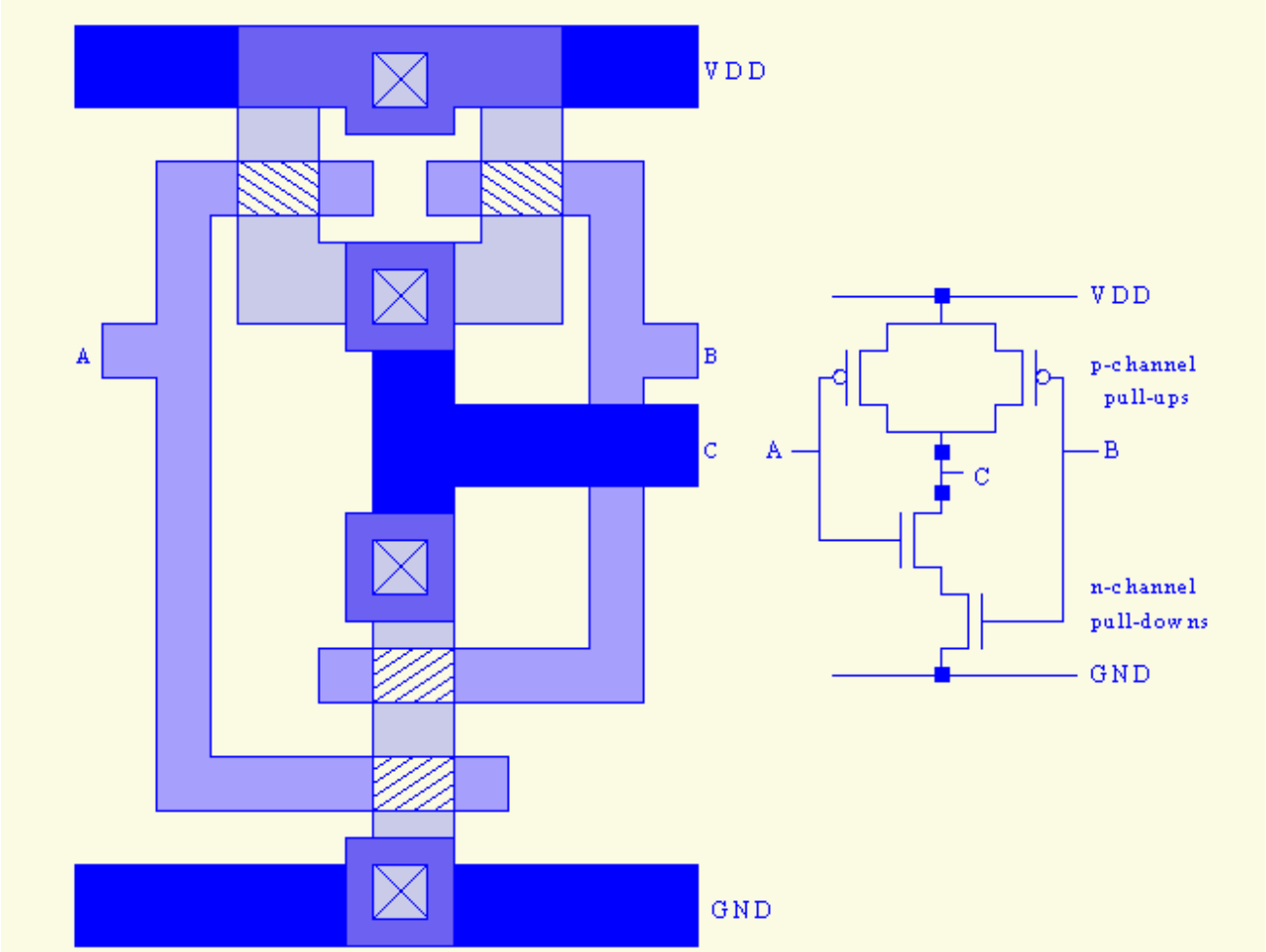
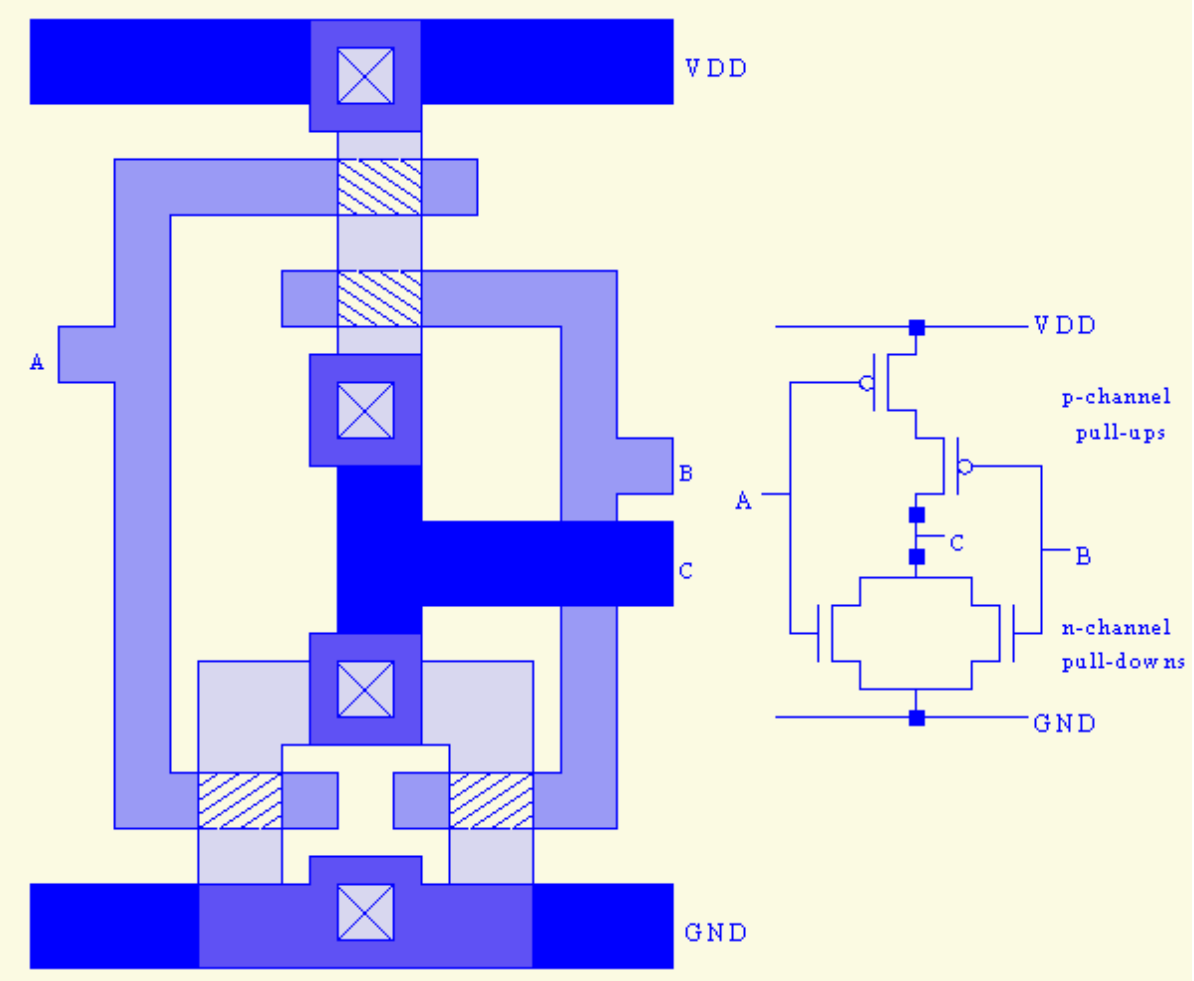
A CMOS Inverter



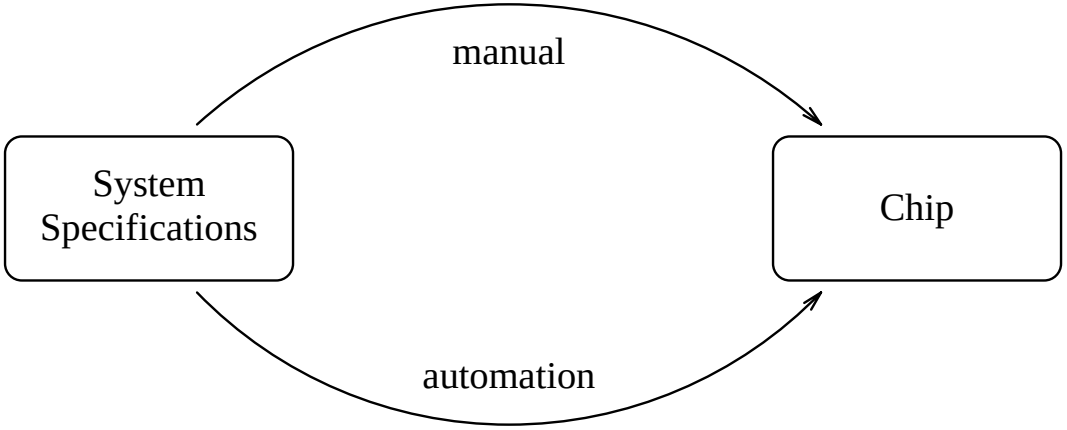
A CMOS NAND Gate



A CMOS NOR Gate



VLSI Design Cylce



- Large number of devices
- Optimization requirements for high performance
- Time-to-market competition
- Cost

ECE6133: Physical Design Automation of VLSI Systems

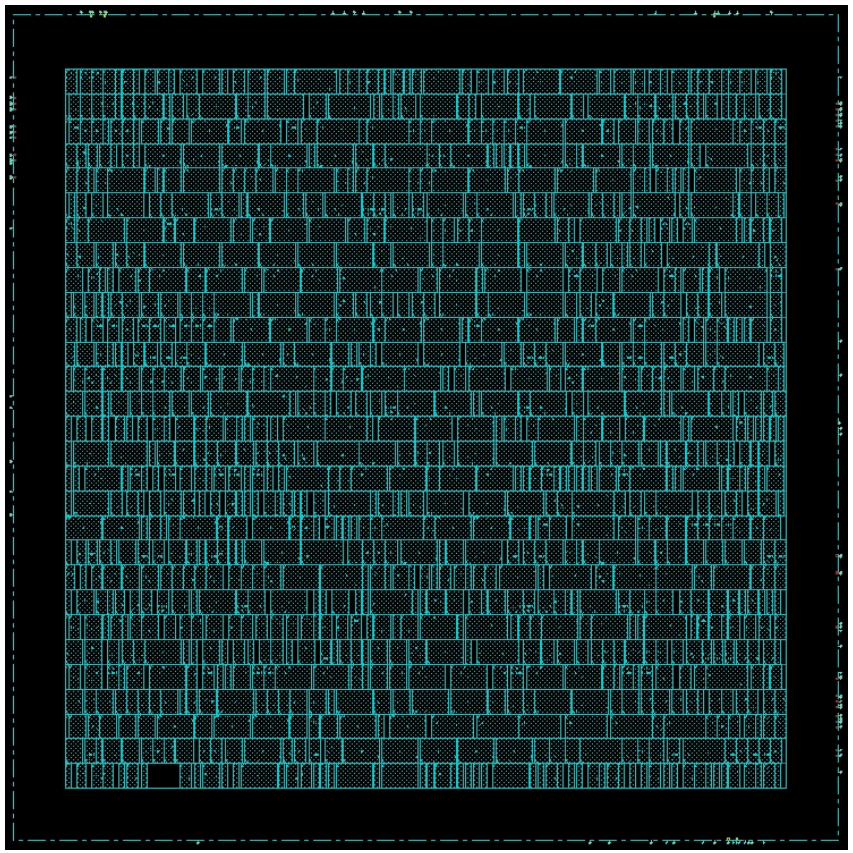
Sample Automatic Layout

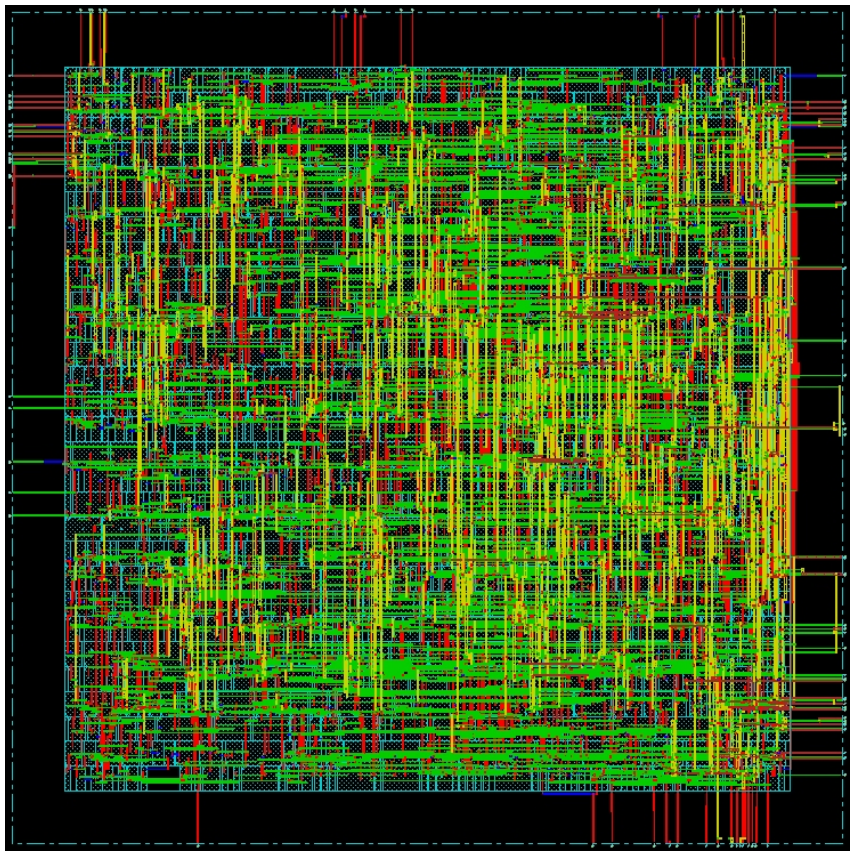
matrix solver
multiply-accumulate (MAC) unit
32-bit processor

Prof. Sung Kyu Lim, Georgia Institute of Technology

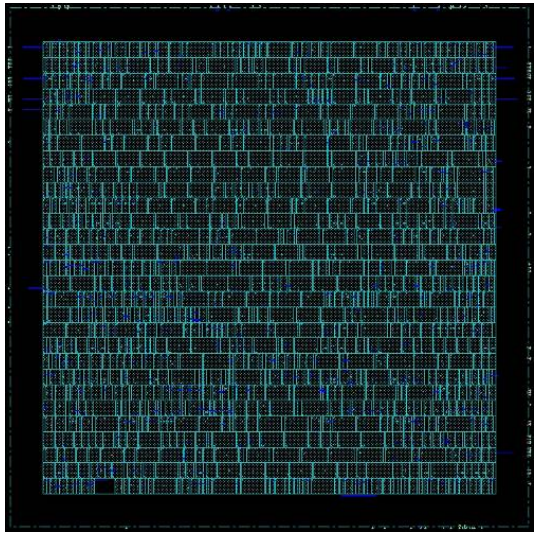
Matrix Solver (20K)

- **Cadence Encounter: placement (1 sec), routing (12 sec)**
  - **Area = 72x72um (45nm library), used 6 metal layers**

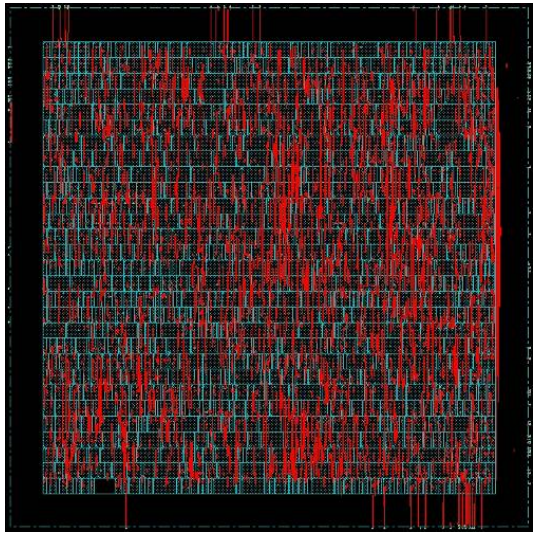




Matrix Solver (20K)



M1



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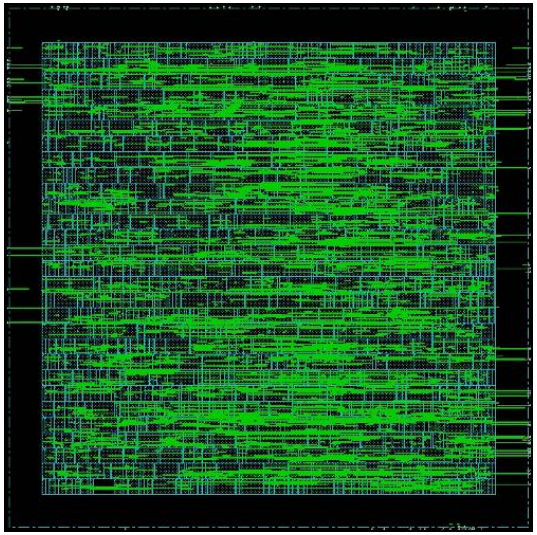
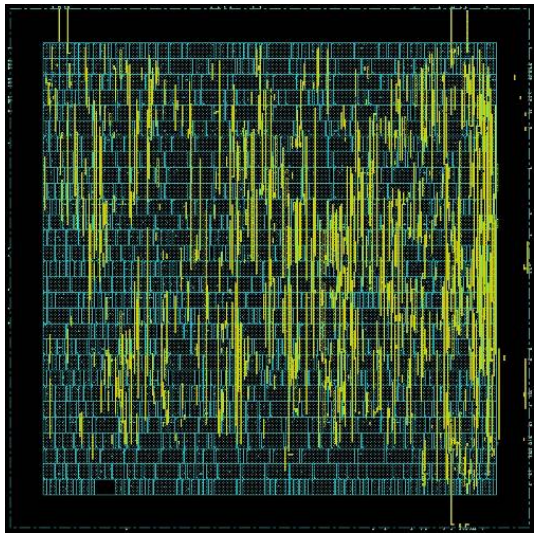
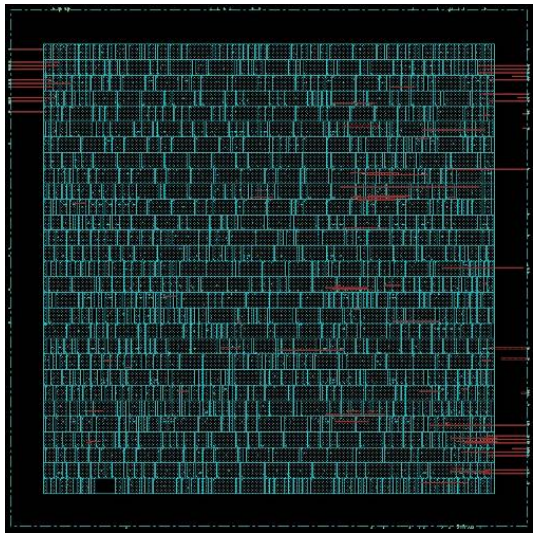


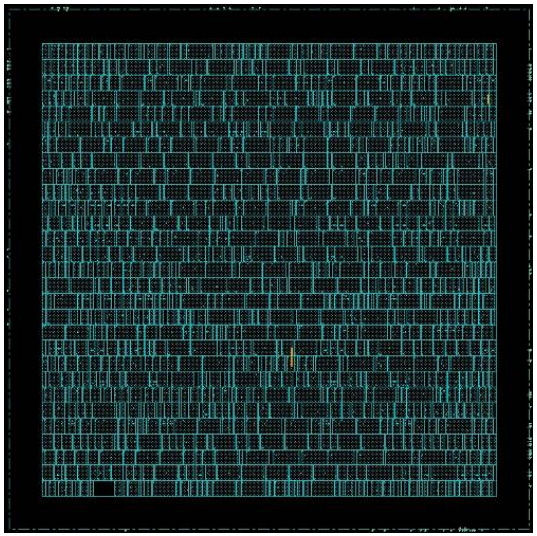
M3



M4



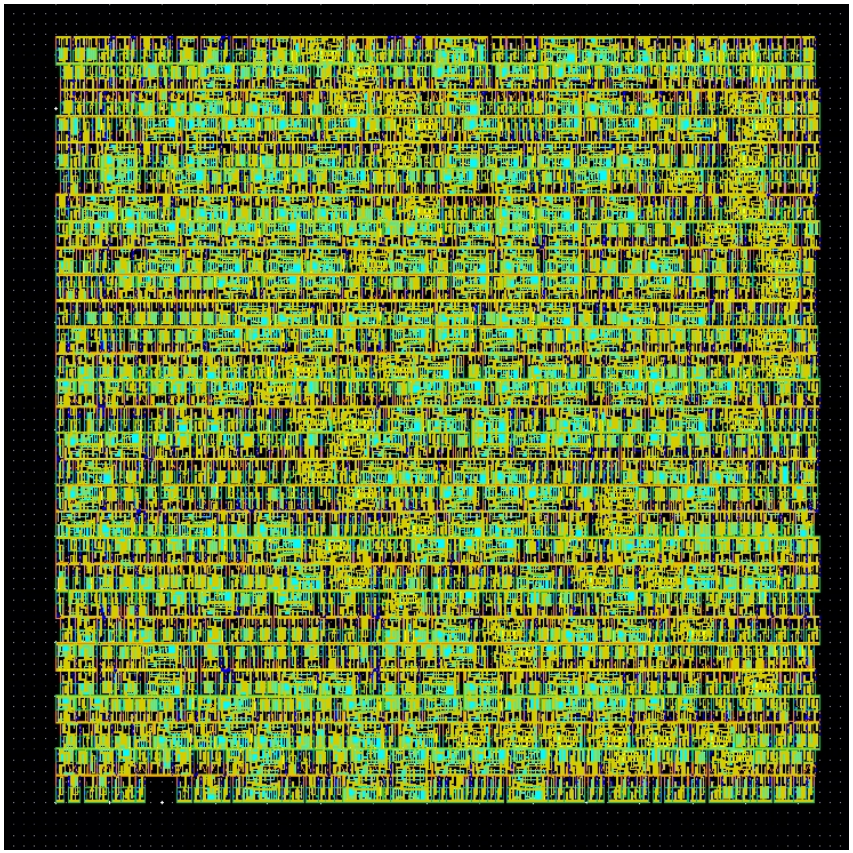
M5

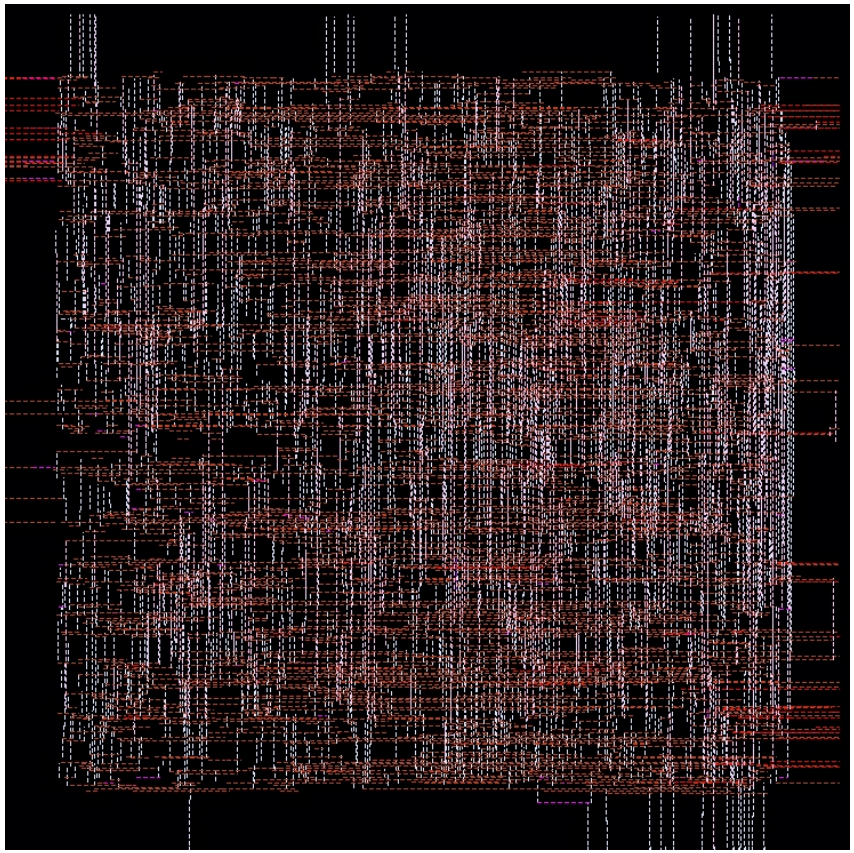


M6

Matrix Solver (20K)

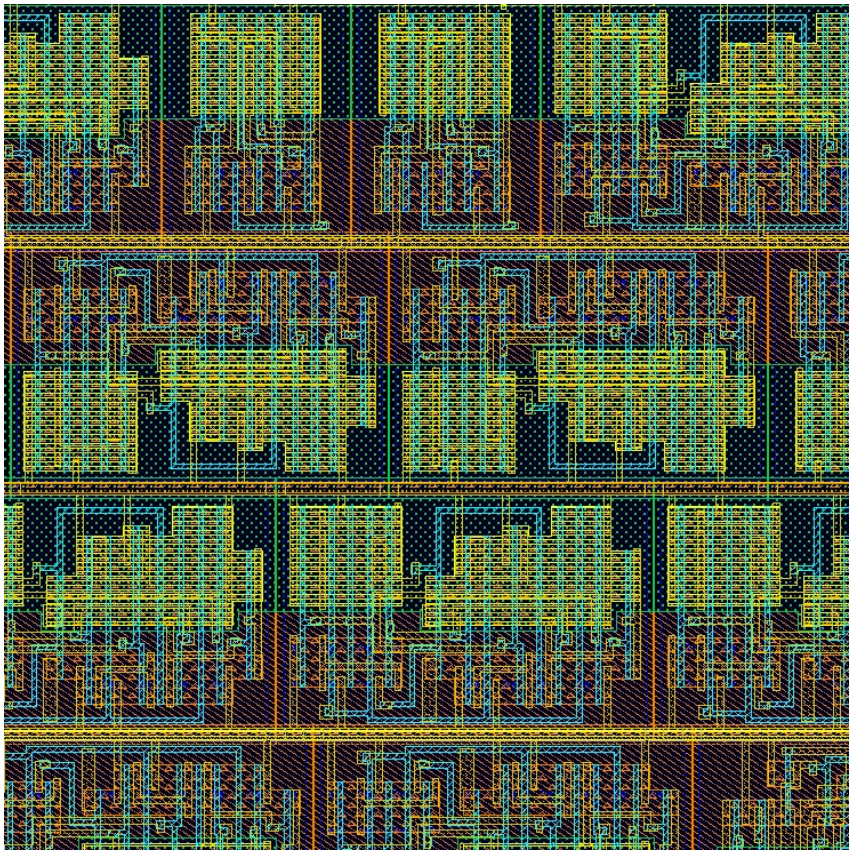
- **GDSII shots: manufacturing-ready**
  - **Used Cadence Virtuoso, passed DRC**

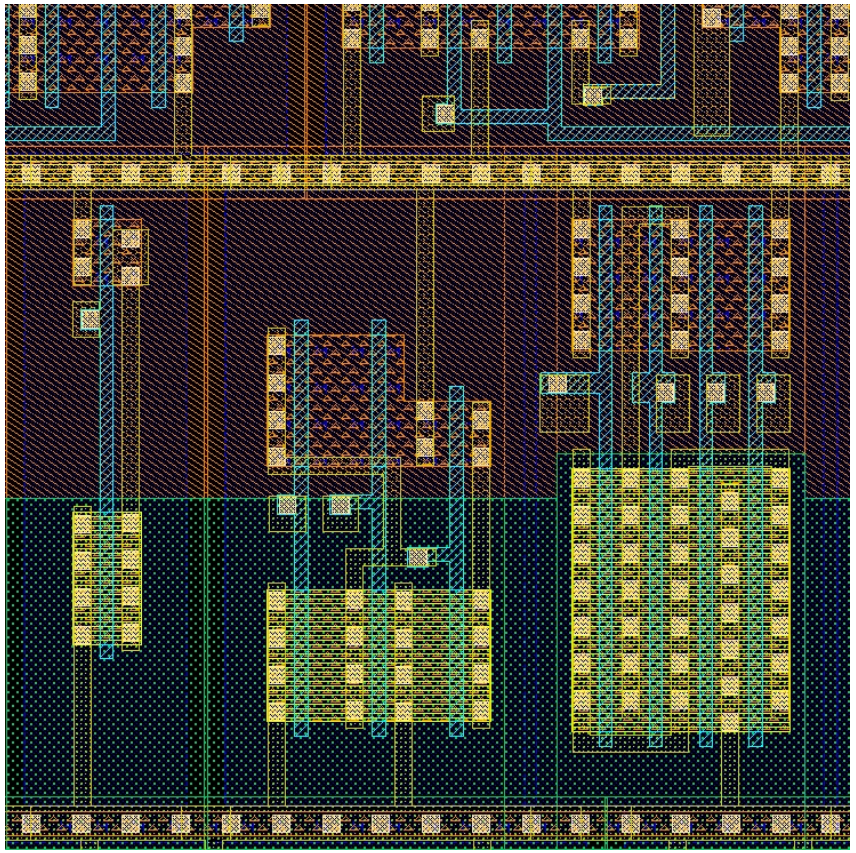




Matrix Solver (20K)

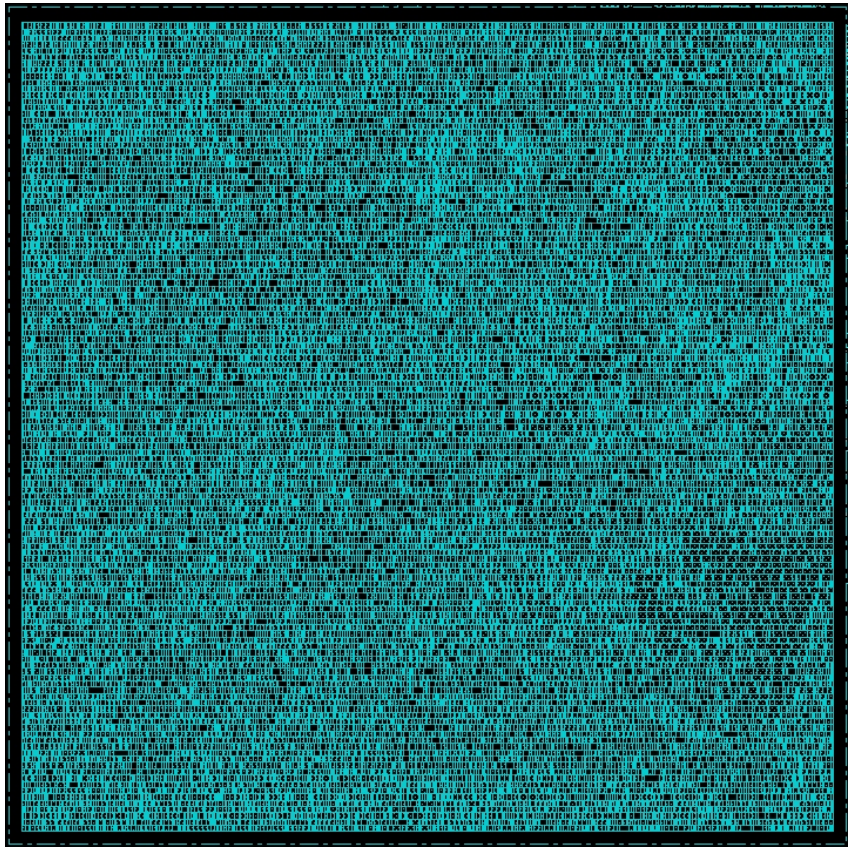
- **GDSII shots: manufacturing-ready**
  - **Specify all intra-cell details**

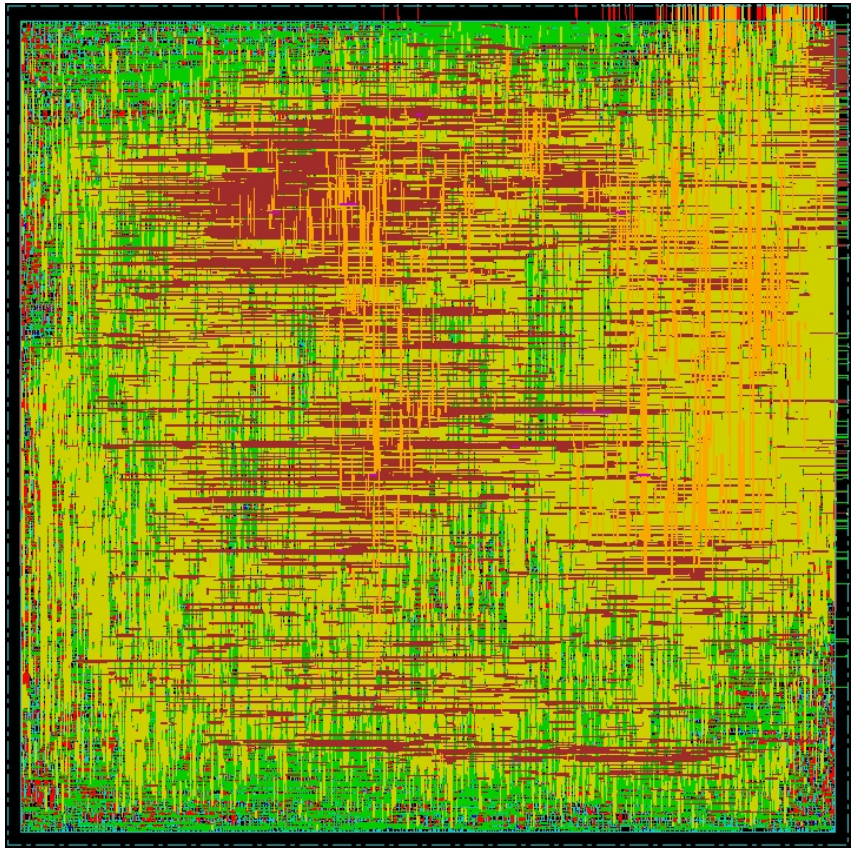




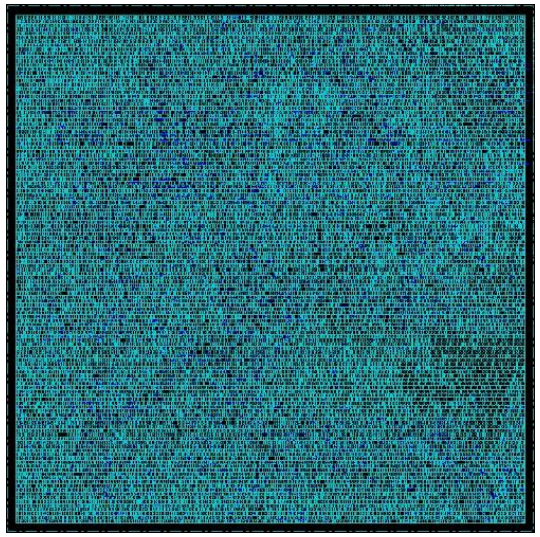
MAC Unit (267K)

- **Placement took 44 sec, routing took 289 sec**
  - **Area = 320x320um, used 7 metal layers**





MAC Unit (267K)



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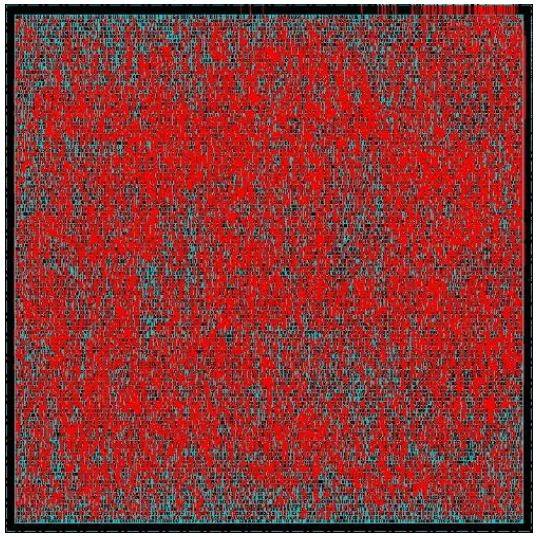

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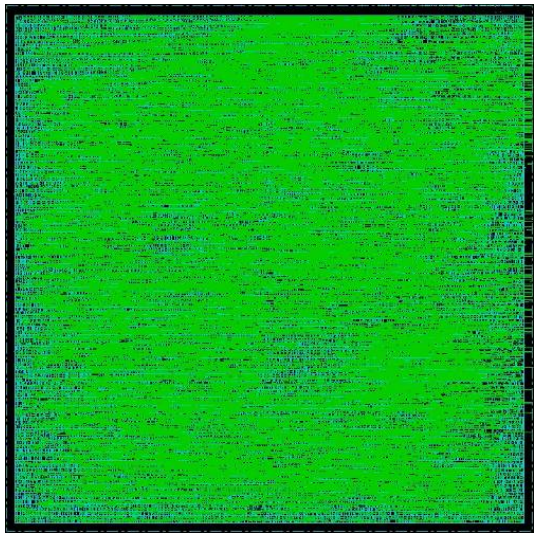
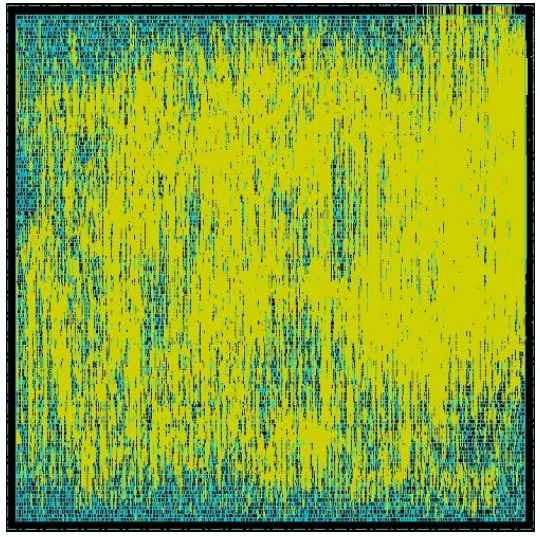
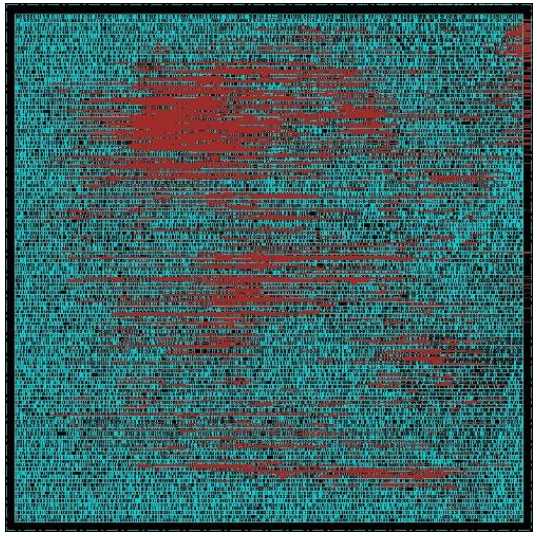


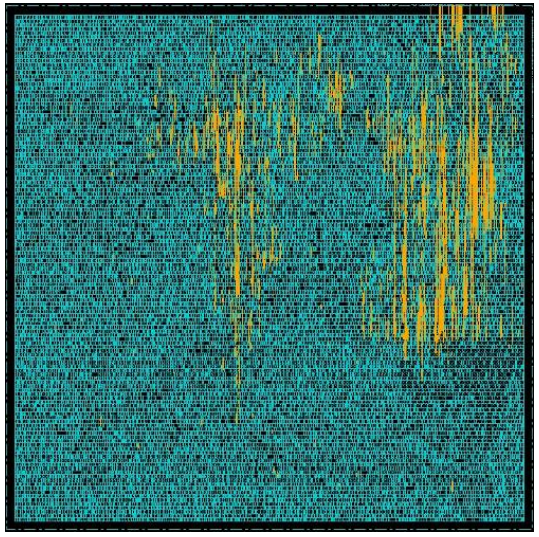
M3



M4

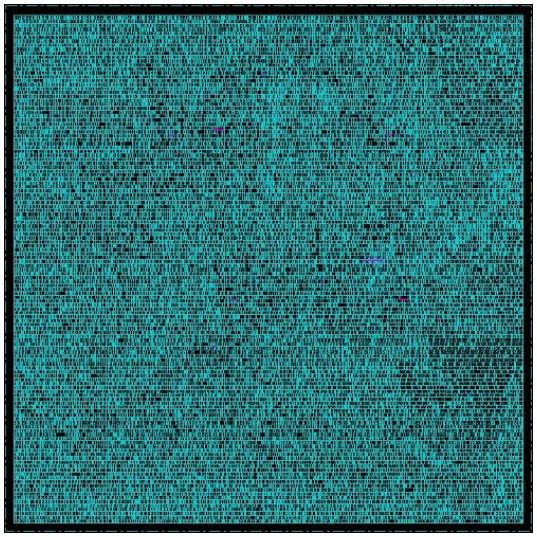


M5



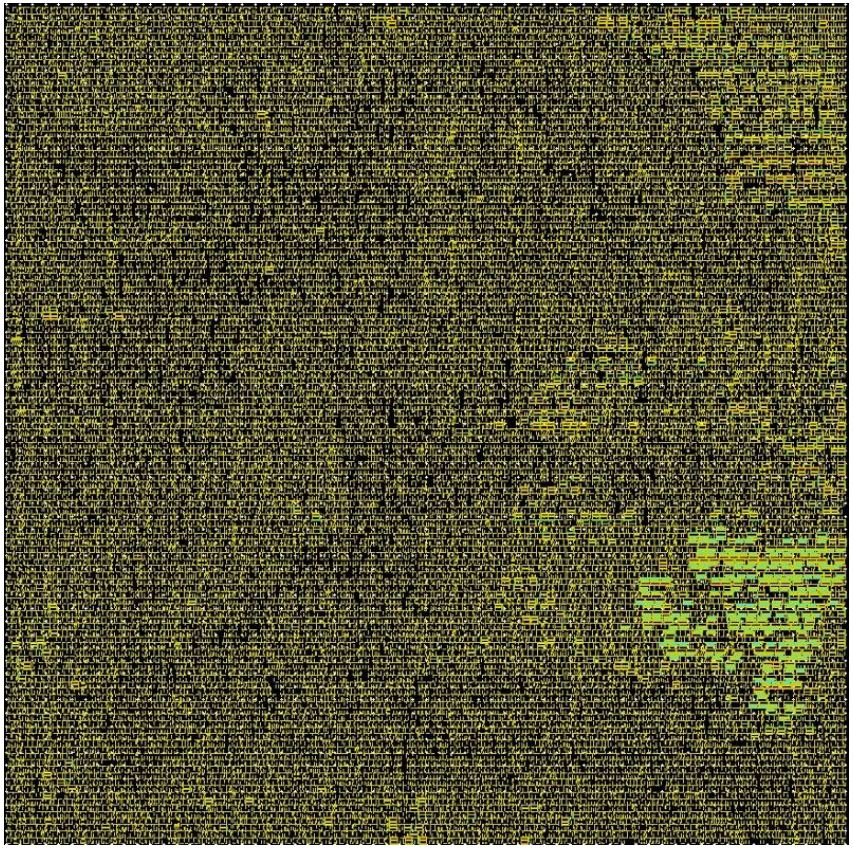
M6

MAC Unit (267K)

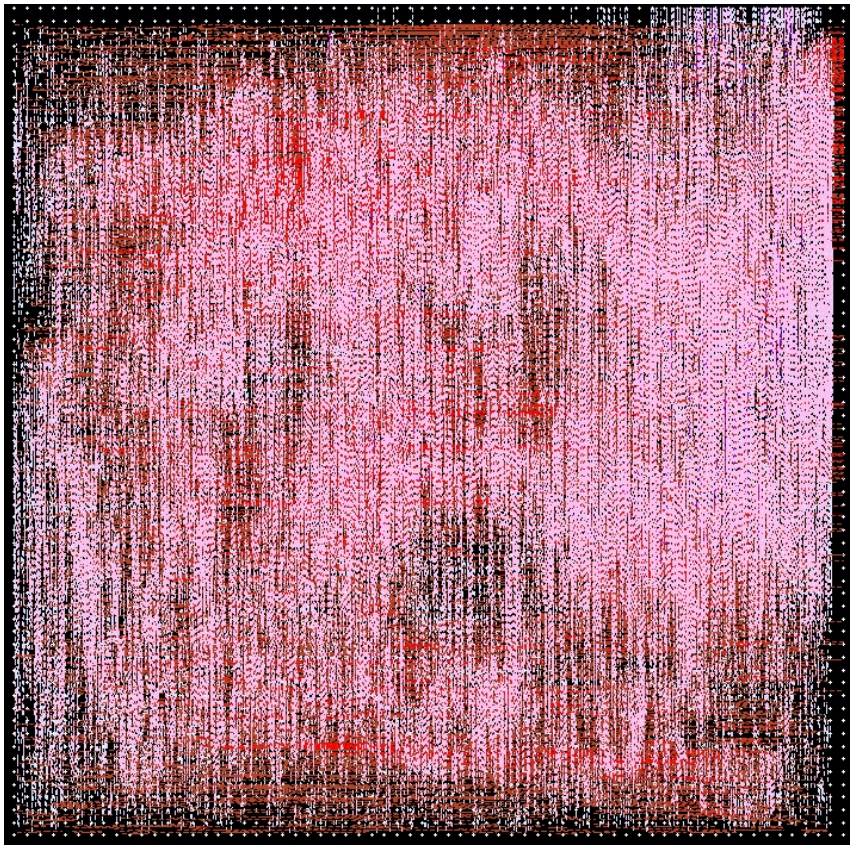


M7

MAC Unit (267K)

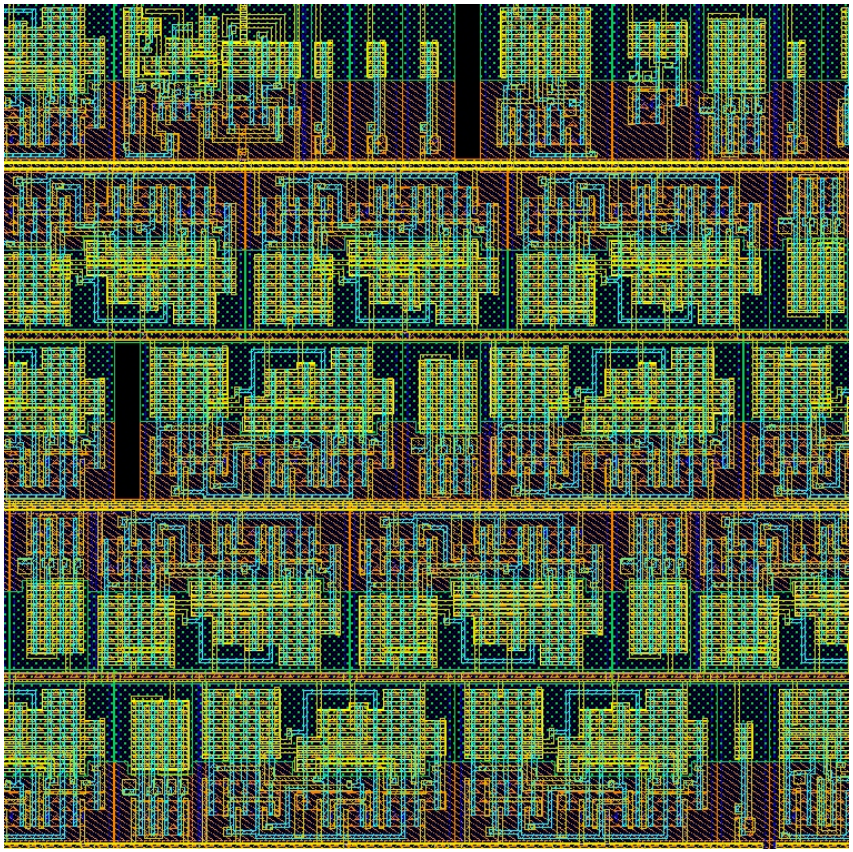


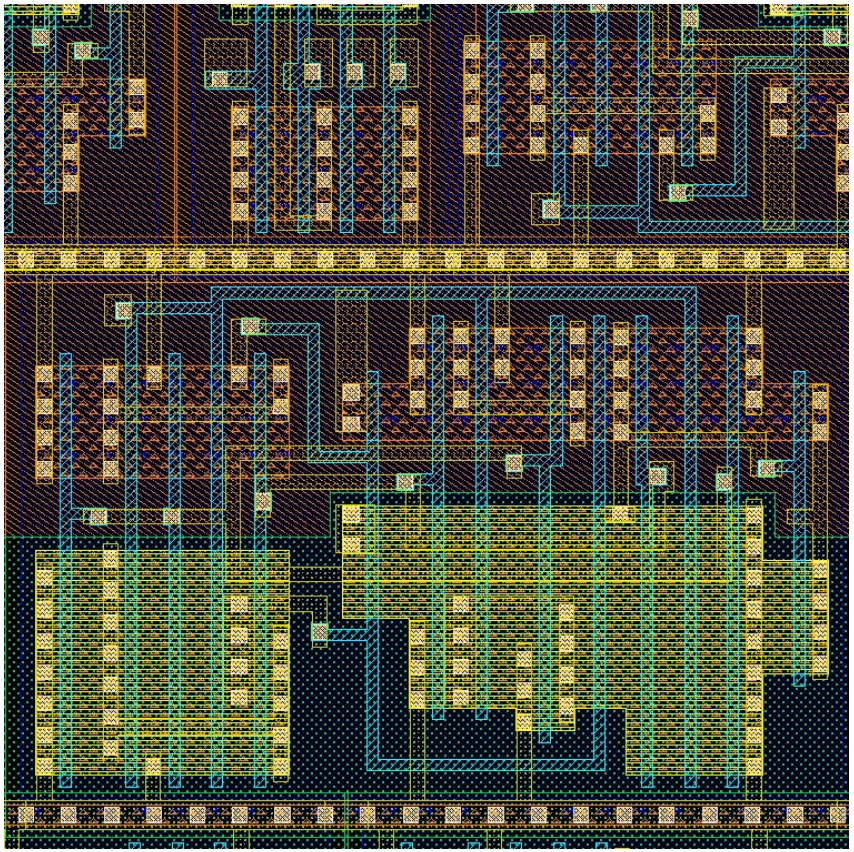
Placement



Routing

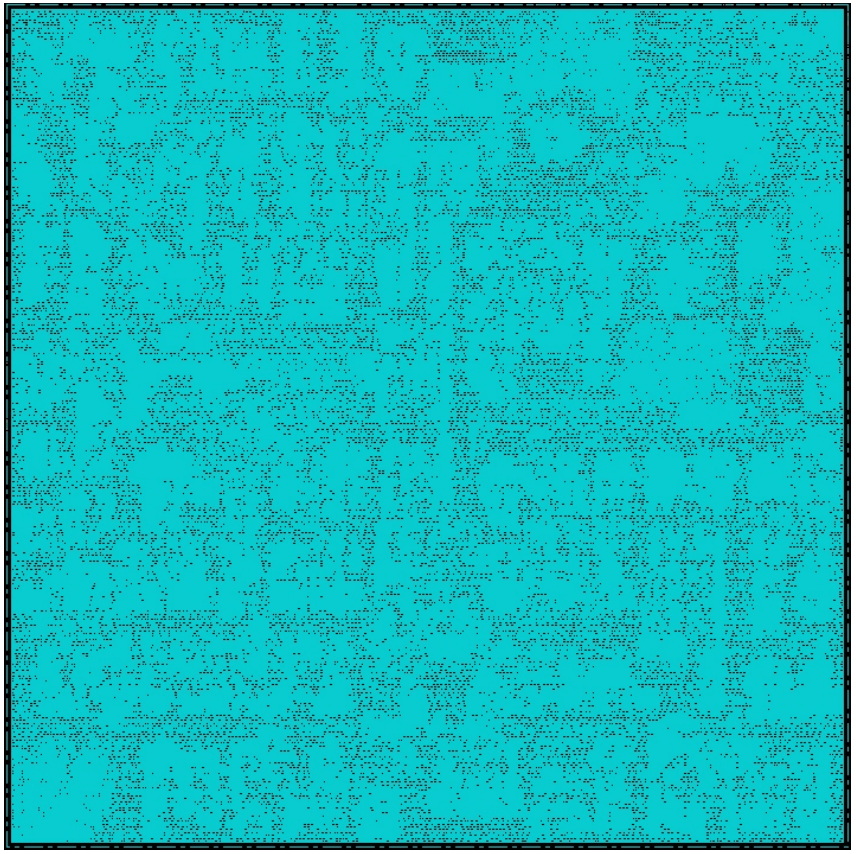
MAC Unit (267K)

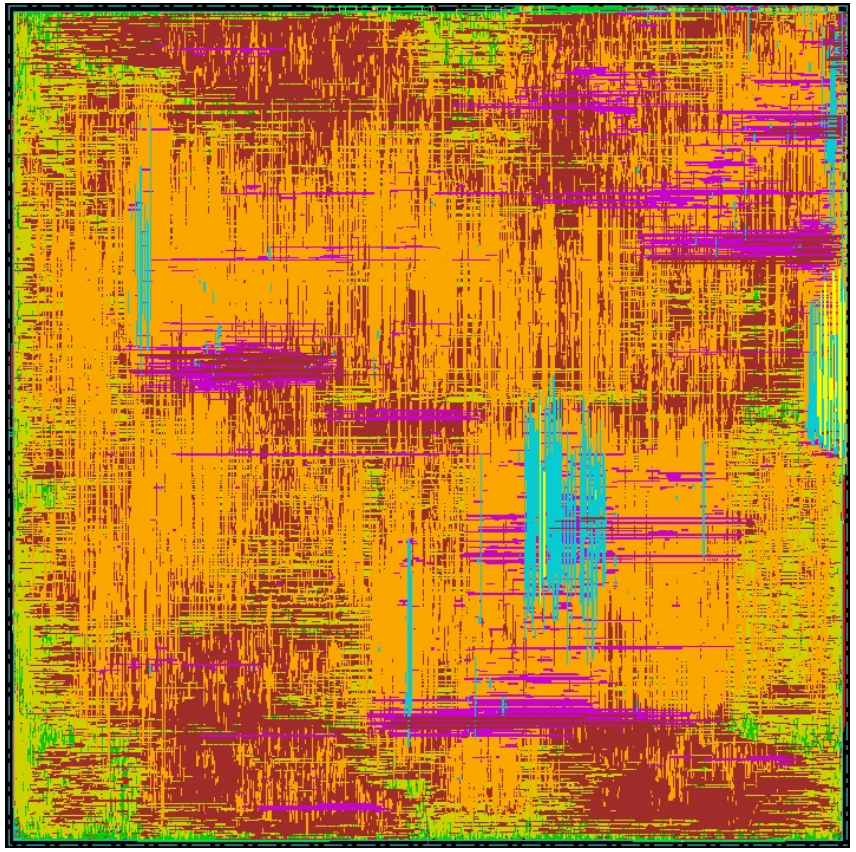




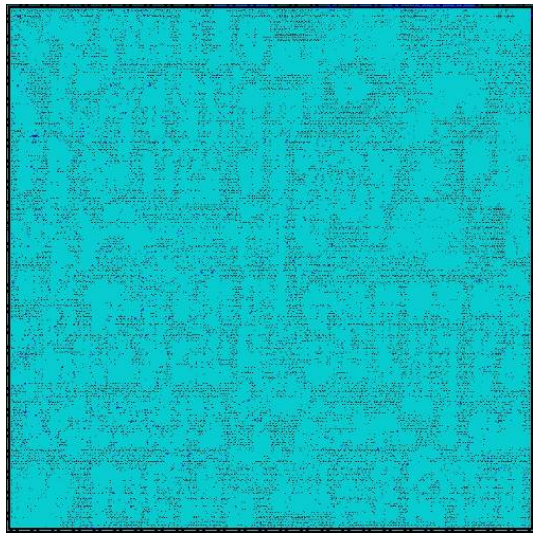
32-bit Processor (2.7M)

- **Placement took 739 sec, routing took 4740 sec**
  - **Area = 1000x1000um, used 10 metal layers**

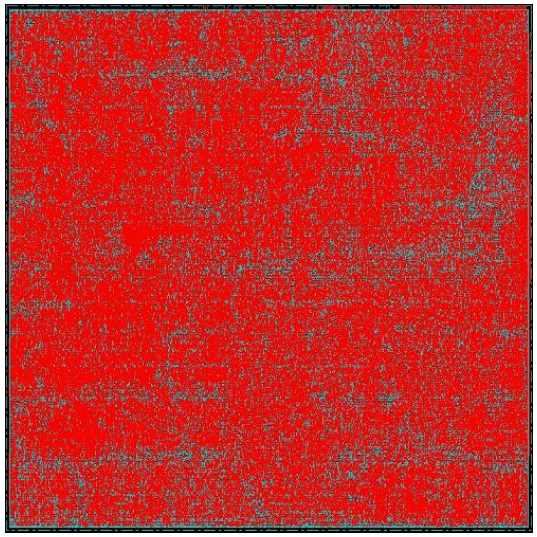




32-bit Processor (2.7M)



M1



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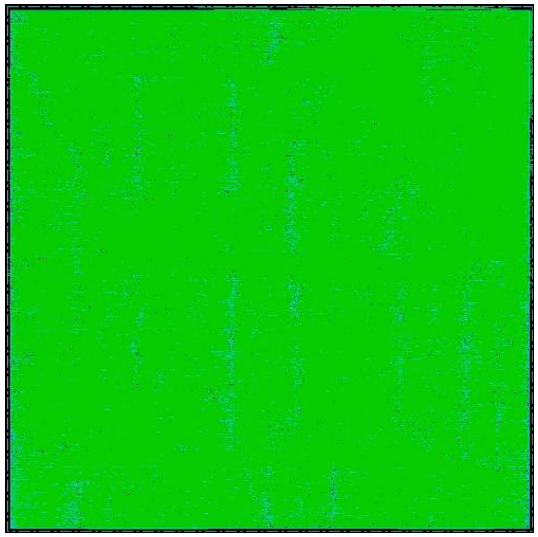

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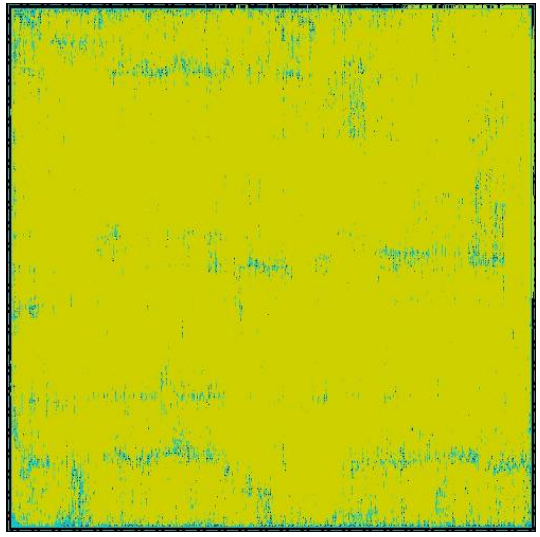
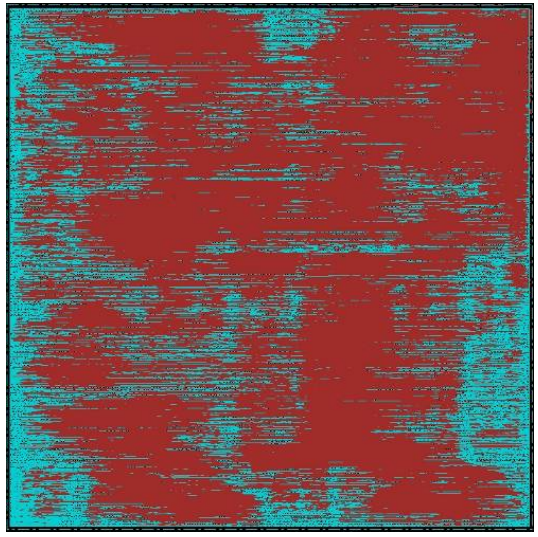
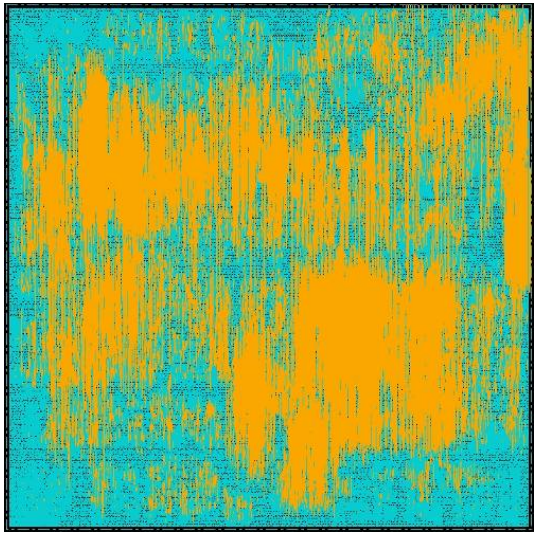


M4

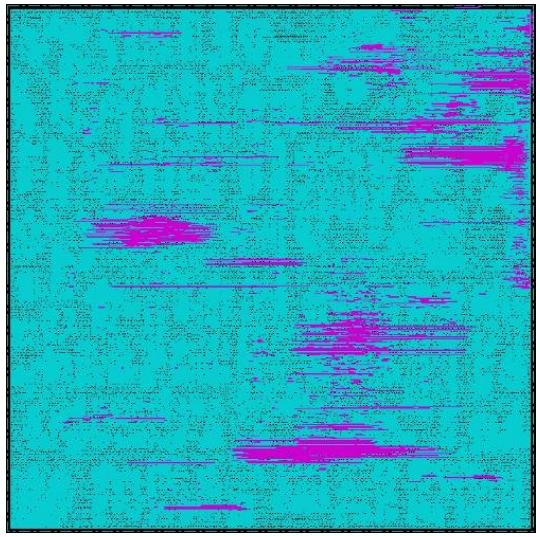


M5



M6

32-bit Processor (2.7M)



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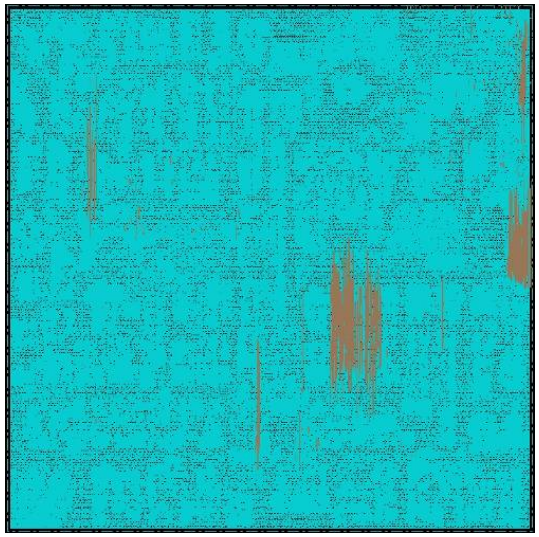

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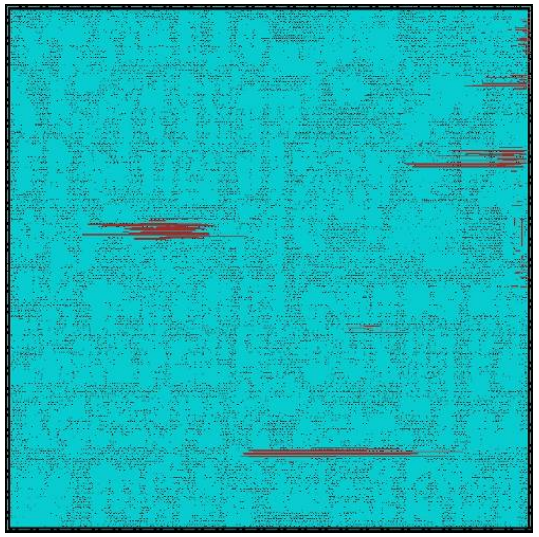
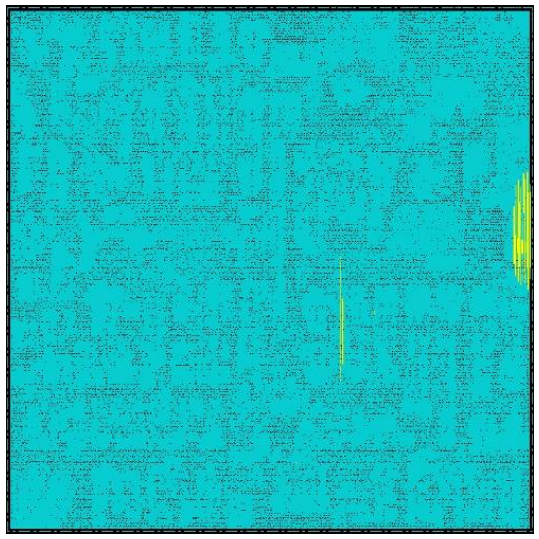


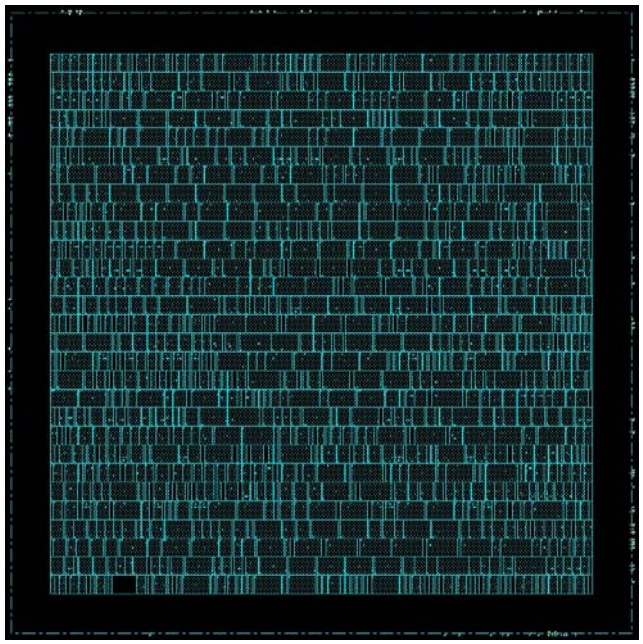
M9



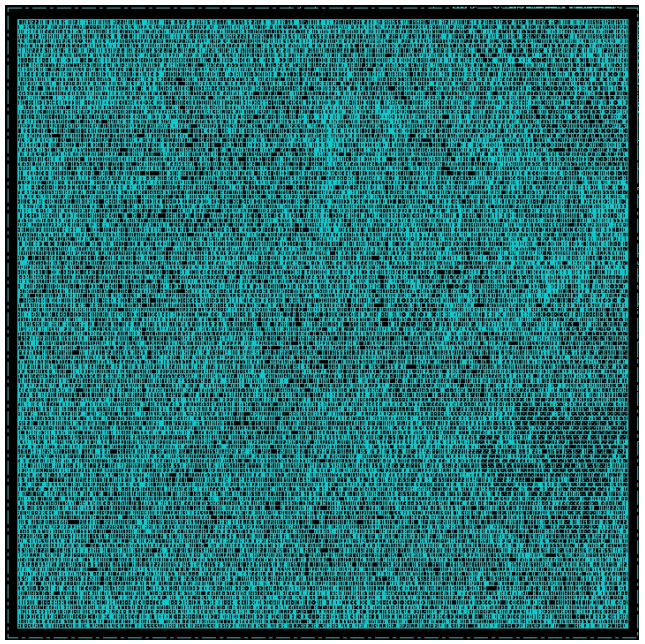
M10

Placement Comparison

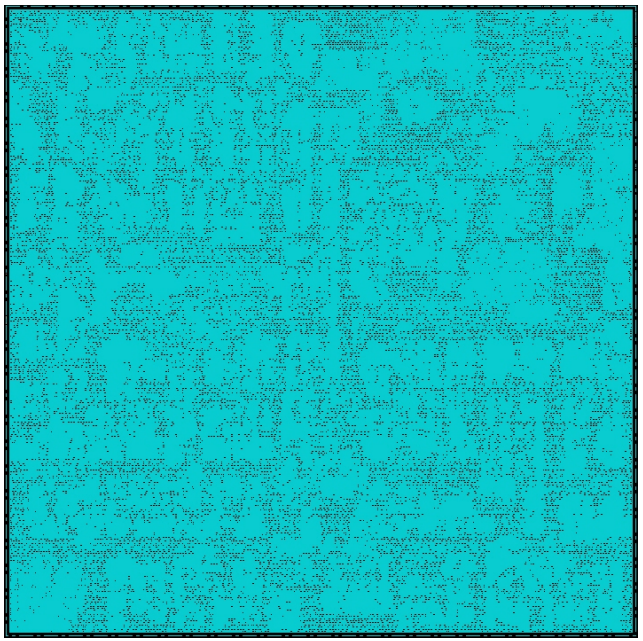
- **Runtime: 1 sec vs 44 sec vs 739 sec**



20K



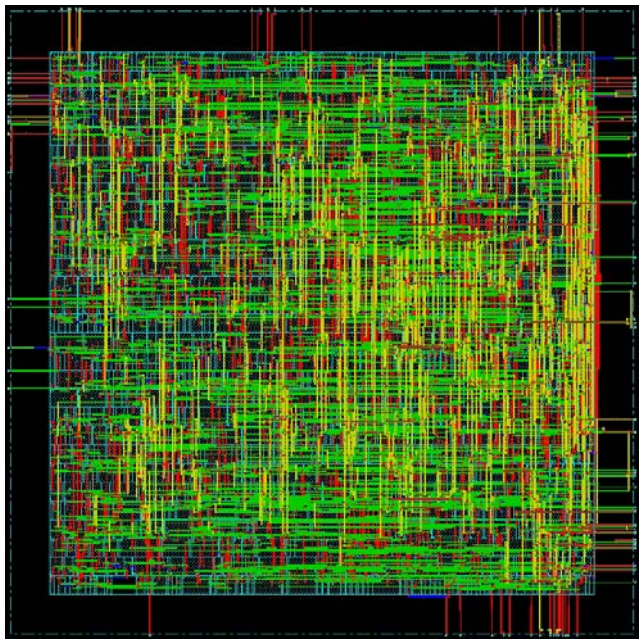
267K



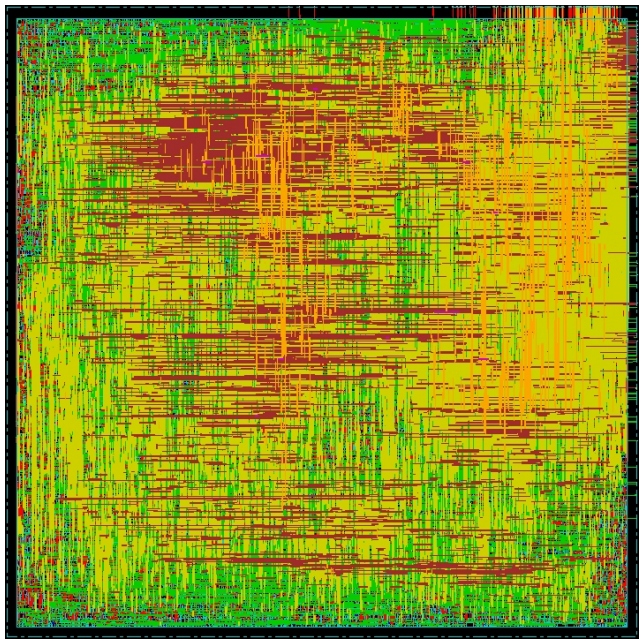
2.7M

Routing Comparison

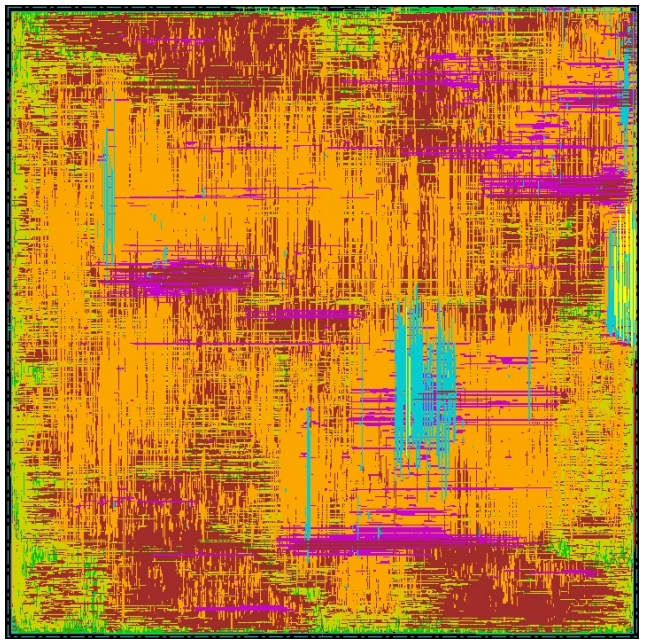
- **Runtime: 12 sec vs 289 sec vs 4740 sec**



20K



267K

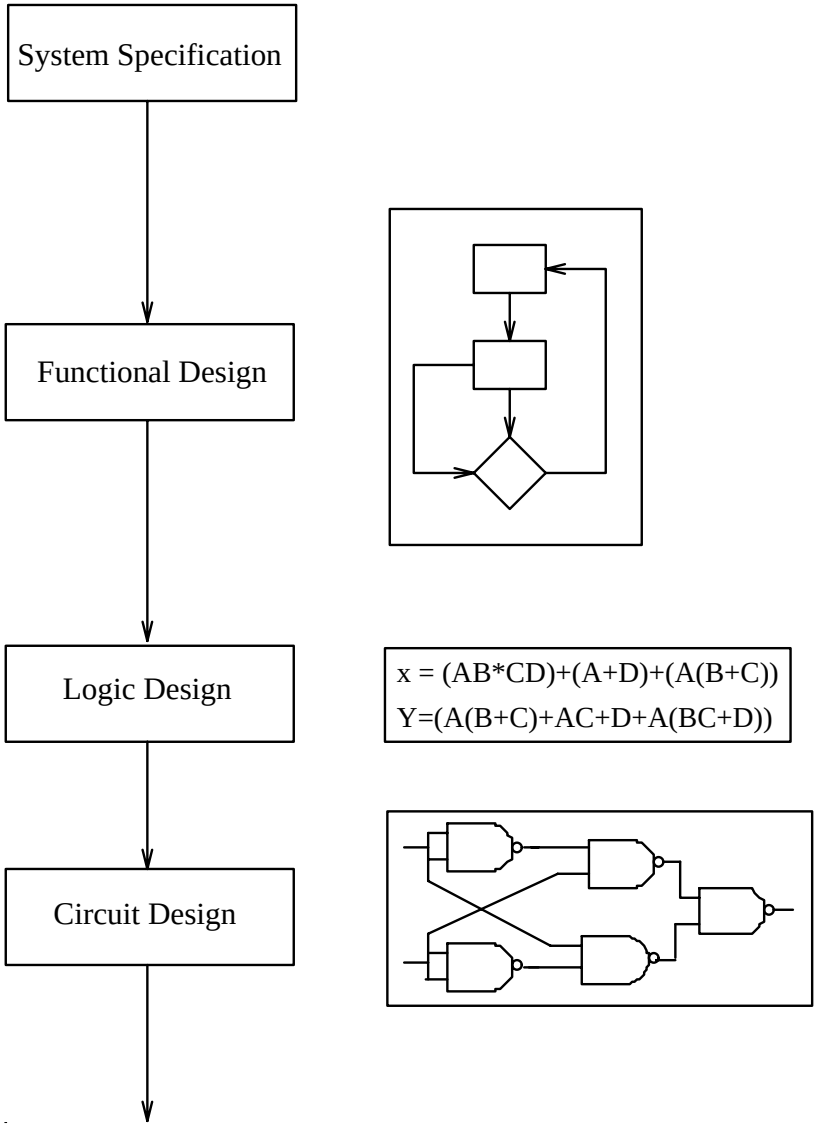


2.7M

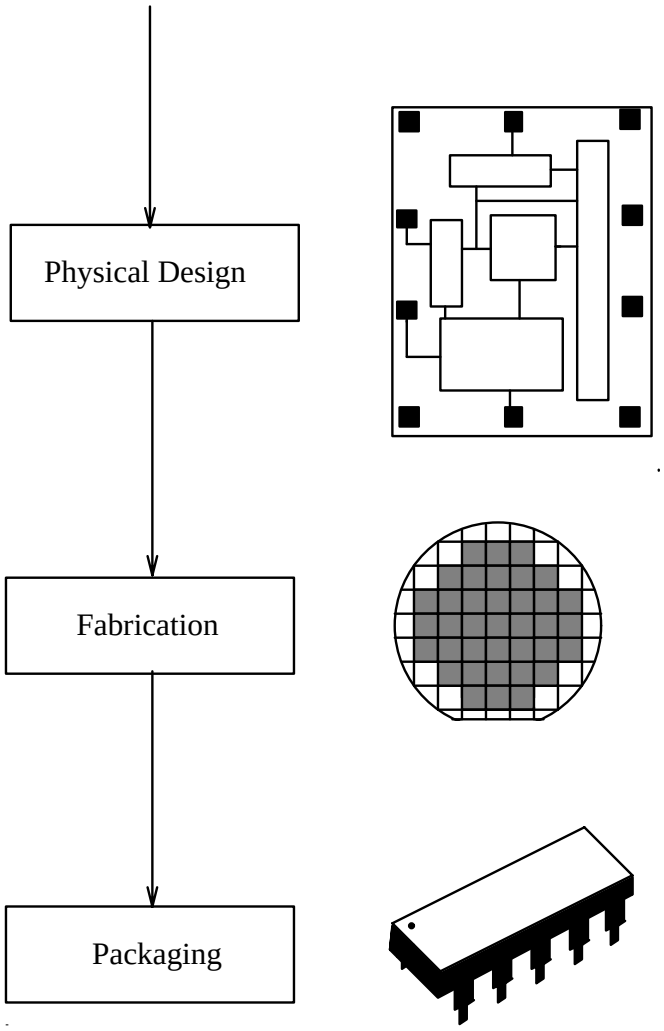
VLSI Design Cycle

1. System Specification
2. Functional Design
3. Logic Design
4. Circuit Design
5. **Physical Design**
6. Design Verification
7. Fabrication
8. Packaging, Testing, and Debugging

VLSI Design Cycle



VLSI Design Cycle (cont.)

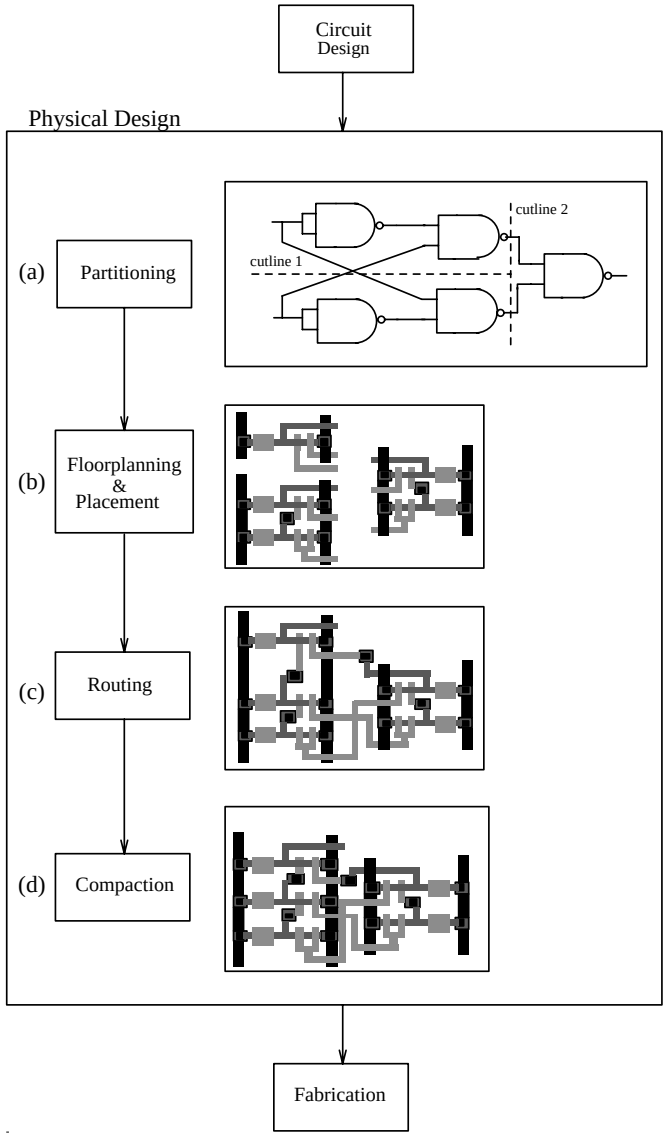


Physical Design

Physical design converts a circuit description into a geometric description. This description is used to manufacture a chip. The physical design cycle consists of

1. Partitioning
2. Floorplanning and Placement
3. Routing
4. Compaction

Physical Design Cycle



Summary

1. Physical design is one of the steps in the VLSI design cycle.
2. Physical design is further divided into partitioning, placement, routing and compaction.
3. There are five major design styles, e.g., full custom, standard cell, gate array, sea of gates and FPGAs.
4. There are three alternatives for packaging of chips, e.g., PCB, MCM and WSI.
5. Automation reduces cost, increases chip density, reduces time-to-market, and improves performance.
6. CAD tools currently lag behind fabrication technology, which is hindering the progress of IC technology.

Setting the Expectations Right

item	
Prior knowledge in algorithms and CAD	Not needed
Class workload	light
Popular (classical and new) physical design algorithms	Covered
Advanced physical design algorithms	Somewhat
Inner workings of algorithms	Covered
In-depth mathematics of algorithms (derivations and proofs)	No
Problem solving homework	Covered
Coding homework	No
Layout design lab	One
Programming project	Optional
Get a job (EDA tool development or chip design)	Yes!

Student Feedback: Steve M.

- I took ECE 6133 in Spring 2019. Along with many other courses, this course gave me the opportunity to join Intel Corporation as an SoC design engineer Intern.

- Most of the work I do at Intel is physical design which is similar to what I studied in ECE 6133. I have also been part of a research team who focused on how to ameliorate their manual routing strategy and was recently offered a full time offer for June 2020.

Student Feedback: Bhargav D.

- I was one of your undergrad students in your Spring 2021 ECE 6133 class. I just wanted to write this email saying thank-you for offering that course project because I got a Summer 2022 internship at Apple as a GPU Physical Design Intern.

- A big part of why I was able to even get an interview with the team is by putting the 6133 project in my resume; the team was very interested in what I did for that and was a good talking point in 2 interviews. I don't think I would've gotten the position if I didn't take your class or do the project.