FPGA, a future proof programmable system fabric

Ivo Bolsens
CTO Xilinx
March 2005
Outline

• State-of-the-art
• Alternatives
• Towards domain optimized programmable platforms
  – Embedded Processing
  – Connectivity
  – DSP
• Domain specific system design flow
• University Interaction
• Conclusions
Where Xilinx Fits

Key components of an digital electronics system:

- Processor
- Memory
- LOGIC

Xilinx: From Inventor of Programmable Logic Device To Leading Innovator in Programmable Digital System Design
Introducing Xilinx

• Leader in fastest growing semiconductor segment
  – Invented programmable chip in 1984
  – > 50,000 design starts/year

• Leader in semiconductor process technologies
  – First to 180nm, 150nm, 130nm and 90nm

• Pioneer of fabless semiconductor model
  – Focus on design, marketing, support
  – Partner for everything else

• A well-managed company and great place to work
  – #4, #5 in Fortune’s 2003, 2004 “Best 100 Places to Work”
Xilinx Product Portfolio

- **Virtex-4**: High Integration, High Performance, Lowest System Cost
- **Spartan-3**: High Volume, Lowest Cost Logic
- **CoolRunner-II**: Highest Volume, Lowest Cost, Lowest Power

Software and Development Tools:
- Xperts
- Alliance
- ISE Development Systems
- WebPACK
- LogiCORE

Support Services:
- Support Services
- Education Services
- Support.xilinx.com
- Design Services
Xilinx Revenue

Fiscal Years


$ Millions

1600 1400 1200 1000 800 600 400 200
Xilinx Revenue Breakdown

Calendar Year 2004

Revenue by Geography

- North America: 42%
- Europe: 20%
- Japan: 14%
- Asia Pacific: 24%

Revenue by End Market

- Communications: 53%
- Storage & Servers: 11%
- Consumer, & Other: 36%

Source: Xilinx, Inc.
The Programmable Marketplace

Calendar Year 2004

PLD Segment
- Actel: 6%
- Lattice: 8%
- QuickLogic: 2%
- Other: 1%
- Altera: 32%
- Xilinx: 51%

FPGA Segment
- Xilinx: 59%
- All Others: 41%

Xilinx revenues are greater than all other pure-play PLD companies combined.

Source: Company reports
Latest information available; computed on a 4-quarter rolling basis
Lattice revenues estimated based on company guidance for Q4CY03 results
Chip Requirements

- **Programmable**
  - mass market of one
- **Regular**
  - manufacturability
- **Scalable**
  - future proof, ride Moore’s law
- **Parallelism**
  - best performance and power
- **Distributed memory**
  - solve data transfer bottleneck
- **Cost optimized**
  - low NRE

“If FPGAs wouldn’t exist, people would have to invent them…”
A Decade of Progress

- 200x More Logic
  - Plus memory, µP, DSP, MGT
- 40x Faster
- 50x Lower Power
- 500x Lower Cost
State-of-the-art Platform FPGA

200,000 Flexible Logic Cells

500 MHz Digital Clock Management

500 MHz, 10Mbits BRAM with FIFO & ECC

700 Mips PowerPC® Processor with Auxiliary Processing Unit and 10/100/1000 Ethernet Mac

0.6-11.1 Gbps Serial Transceivers

500 MHz Programmable DSP Execution Units

AES Design Encryption

1 Gbps Source Synchronous I/O
Highest FPGA Performance

- I/O LVDS Bandwidth: 480 Gbps
- I/O Memory Bandwidth: 260 Gbps
- High-speed Serial I/O: 10 Gbps
- On-chip RAM Speed: 500 MHz
- DSP: 500 MHz, 702 DMIPS
- Logic Fabric Performance: Breakthrough Performance

Performance Chart:

- I/O LVDS Bandwidth
- I/O Memory Bandwidth
- High-speed Serial I/O
- On-chip RAM Speed
- DSP
- Logic Fabric Performance
The Platform FPGA

- MGTs
- Logic Emulation
- DSP
- Memory
- PowerPC
- I/Os
- Communication Port
- Custom Logic
- DSP Accelerator
- Internal Memory
- μP
- External Memory Port

Georgia Tech
System Platform Example

CDMA2000 “Converged” Base Station

Customer Benefits:
- High performance Gigabit Transceivers
- Integration of PowerPC processors
- HW/SW partitioning/flexibility

- XtremeDSP Signal Processing for Wireless Algorithms
- Embedded PowerPC Processing For Call Management and System Control
- RocketIO Gigabit Serial for System Interconnect
- RocketIO Gigabit Serial for System Intraconnect

Next-Gen CDMA2000 Wireless Basestation
Benefits of Configurability

<table>
<thead>
<tr>
<th>Where</th>
<th>Why</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Vendor</td>
<td>FPGA Economics</td>
</tr>
<tr>
<td>System Designer</td>
<td>Design Verification</td>
</tr>
<tr>
<td></td>
<td>Edit/Compile/Debug</td>
</tr>
<tr>
<td>System Manufacturer</td>
<td>System Test</td>
</tr>
<tr>
<td>Field</td>
<td>Power-up</td>
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<tr>
<td></td>
<td>Self Test</td>
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<td></td>
<td>Customization</td>
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<td></td>
<td>Field Upgrade</td>
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<td></td>
<td>Evolvable Systems</td>
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</tbody>
</table>
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The Processor Platform

Viktor Peng, MIPS
The ASIC/ASSP Platform

Cost increases over previous generation:

<table>
<thead>
<tr>
<th>Component</th>
<th>Increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design</td>
<td>60%</td>
</tr>
<tr>
<td>Manufacturing</td>
<td>40%</td>
</tr>
<tr>
<td>Mask Costs</td>
<td>100%</td>
</tr>
</tbody>
</table>

Building a next generation SoC ASIC (90nm?):

<table>
<thead>
<tr>
<th>Cost</th>
<th>Amount</th>
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</thead>
<tbody>
<tr>
<td>Development Cost</td>
<td>$30-50M</td>
</tr>
<tr>
<td>Total Cost of bringing product to market</td>
<td>$80M</td>
</tr>
<tr>
<td>Revenues needed to breakeven in 2 yrs</td>
<td>$150M</td>
</tr>
</tbody>
</table>

- 2007 ASIC/ASSP forecast = ~$80B
- ~500 successful ASIC/ASSP design starts
  - NRE $30M, R&D 20% of revenue, $150M revenue

* Source Dataquest, IBS, Xilinx
FPGA- ASIC/ASSP Crossover

- 90nm / 300mm ASICs
- 150nm / 200mm ASICs
- 150nm / 200mm FPGAs
- 90nm / 300mm FPGAs

**FPGA Cost Advantage**

Production Volume → Cost
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Domain Optimized Platforms

One Family – Multiple Platforms

Column based features

- Logic
- Memory
- DSP
- Processing
- High-speed I/O

Virtex-4 LX

Logic Domain
Highest logic density

Virtex-4 SX

DSP Domain
Highest DSP performance

Virtex-4 FX

Connectivity Domain
Embedded Processors
High-speed Serial I/O

- Enables “Dial-In” hard IP Mix
  Logic, DSP, BRAM, I/O, MGT, DCM, PowerPC
- Enabled by Flip-Chip Packaging
  I/O Columns Distributed Throughout the Device

XILINX
Both Hard & Soft IP Necessary for Programmable Systems

Programmable hard IP
- Up to 10x less area
- Up to 10x lower power
- Up to 2x performance

Customizable soft IP
- Most flexible
- Widest selection

<table>
<thead>
<tr>
<th>IP</th>
<th>Hard</th>
<th>Soft</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing</td>
<td>PowerPC</td>
<td>Peripherals</td>
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<tr>
<td>DSP</td>
<td>DSP slice (MAC)</td>
<td>Accelerators, Additional µPs</td>
</tr>
<tr>
<td>Connectivity</td>
<td>PHY (ser./par.)</td>
<td>Algorithms</td>
</tr>
<tr>
<td></td>
<td>Timing critical I/O</td>
<td>Protocols</td>
</tr>
<tr>
<td></td>
<td>logic &amp; clocking</td>
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</tbody>
</table>

Example: Virtex-4 FX platform FPGA
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From Soft to Hard IP

- Range of processing solutions

Soft MicroBlaze
150DMIPS
45 cents
200 in single FPGA

Plus: A broad range of common peripherals and IP
Accelerate Performance Beyond the Processor Core

- New Auxiliary Processing Unit (APU)
  - Direct interface from CPU pipeline to FPGA logic
  - Simplifies integration of Coprocessor and hardware accelerators

- Reduce number of bus cycles by factor of 10X
Close integration HW/SW

• CPU centric Paradigm:
  – CPU is the brain of the system
  – All the execution units are in the CPU
  – The rest of the system resources are storage or IO for the processor and at its disposal.
  – CPU resources are designed to be used only by the CPU

• New Paradigm:
  – The programmable fabric claims some of the responsibility
    • Some Execution Units are implemented in the fabric
  – Soft blocks can use the resources in the CPU
  – The execution flow in the fabric and the CPU have direct coupling

*New APU interface facilitates this and is a step in this direction*
Use model: Coprocessor

Floating Point Unit

![Diagram of Floating Point Unit]
Comparison with Traditional Bus-based

**APU**
- Processor Block
- Write Instruction and operands: 1 APU cycle
- Execution: $N_{EX}$ APU cycle
- Read Result and Status: 1 APU cycle + 1 CPU cycle

**PLB**
- Processor Block
- Write Operand1: 5 PLB cycles + 2 CPU cycles
- Write Operand2 and Instruction: 5 PLB cycles + 2 CPU cycles
- Execution: $N_{EX}$ PLB cycle
- Read Status: 6 PLB cycles + 3 CPU cycles
- Read Result: 6 PLB cycles + 3 CPU cycles
Use Model: Streaming

Processor Block

Control

Operation

Soft Auxiliary Processor

Stream of Data

Data

Instructions

Status
Embedded Design Methodology

- Support HW, SW and mixed HW-SW design using domain-specific as well as a unified tool chain

- Supporting both ends of the usage spectrum provides all points in between as well.
Single Environment For HW and SW Development

- HW and SW Platform generators based on the Xilinx on the Platform Specification Format for programmable systems
- Tight coupling enables a customized SW platform to be generated that matches the customized HW platform
Board Support Package

- Initializes the processor system at power up
- Interfaces between RTOS and the peripheral device
- The drivers are designed to be portable across processor core and RTOS
  - Allows reuse = higher quality
- Integrates the driver into RTOS
- Satisfies the "plug-in" requirements of RTOS
- Needs to be rewritten for each OS

- Initialization Code
  - Initializes all parameters (e.g., MMU, int/ext reg)
  - Initializes the processor system at power up

- Boot Code

- Ethernet 10/100 Device Driver
- UART 16550 Device Driver
- IIC Master & Slave Device Driver
- ATM Utopia Level 2 Device Driver
- Peripheral n, n+1... Device Drivers
Built for Debug

- FPGA fabric provides full internal visibility
- Debug occurs at system speeds
- Never too late in an FPGA
  - Hardware problems can be fixed during development and after product deployment
- Enables on-chip co-verification
  - As part of design process
DSP Sweet Spot - Performance

- ASICs/ASSPs
- Performance
- Low Unit Cost: Most Important
- Flexibility: Most Important
- FPGA Sweet Spot
- DSP Processors

1 MSPS
300 MSPS
The DSP ‘LUT’

18x18 Multiplier

48-bit accum

Op Reg

500MHz

Available on all Virtex-4 Platforms
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Domain Specific Characteristics

• Networking perspective
  – The racing track pit stop
  • lots of concurrent threads (=engineers), on individual packets (=cars)

• DSP perspective
  – The manufacturing line
  • Lots of data tokens (=cars), processed in a pipelined fashion (=dataflow)

• Processor perspective
  – Human operator
  • Central control (=human), accelerators (=tools)

Different application domains require different methodologies to exploit capabilities hardware
DSP domain

Concepts that are familiar to the DSP designer

- Library-based, visual data flow
- Seamlessly integrated with Simulink and MATLAB
- Automatic code generation
  - Synthesizable VHDL
  - IP cores
  - HDL test bench
  - Project and constraint files
Networking: the Click front-end

Each box is a simple processing element
packets flow through
Object Oriented

(Click: MIT, 2001)
Future: API

Design automation tools for system experts (entry, debug, ...)

Provide concurrency, interconnection and programmability

API access

Soft platform template

Exploit concurrency, interconnection and programmability

Efficient mapping

Programmable logic devices

Hooks for existing IP cores and software
Major API components

- **Threads**: lightweight concurrent message processing entities compiled to PLD implementations
- **Hooks**: wrappers for existing functional blocks with PLD implementations
- **Interfaces**: for moving messages into or out of the system perimeter
- **Memories**: for storage of messages, system state or system data
Future : Transparent HW/SW

Search Slot → Backup state → Start Reconfiguration → Restore state

Module A
Module B
Module D
Module E

Bus-Macro
Bus Com 0
ID 0

Bus Com 1
ID 1

Bus Com 2
ID 2

Bus Com 3
ID 3

Run-time Module Controller
µController

End address
State - Data

CAN-Interface
I/O (e.g. CAN)

Decompressor Unit (LZSS)

ICAP

Bootstream

Flash-Memory

Slotstreams

M_A  M_B
M_C  M_D
Future: The Programmable Systems Platform

- Very High-Performance DSP
- High-Speed Serial
- FPGA Users Base
- Embedded Processing
- Next Generation
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• **Future : University Interaction**
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Innovation depends on people

- People and innovation are among our most important assets
- Xilinx believes that people and innovation only thrive when actively nurtured
- Our business actions reflect this belief
- We value long-term, strategic relationships with top academic institutions to support teaching and research programs
Xilinx Research Labs and Xilinx University Program (XUP)

- Xilinx University Program and Research Labs report directly to the CTO
- Seeking a good “impedance match” with university partners
- Xilinx University Program manages donations to Universities
- Xilinx Research Labs manages external research partnerships
XUP supports education

- Logic design
  - Integrated software environment (ISE)
- Embedded systems development
  - Embedded development kit (EDK)
- Digital signal processing
  - System Generator (SysGen)
- Free workshops for professors/students
- PLDs, boards and development systems
www.digilentinc.com

Make any desktop a digital design lab!

Digilent offers products and services to help digital design engineers gain new skills or advance new designs.

Our products include circuit boards that feature Xilinx programmable chips, and peripheral boards that contain a variety of analog and digital I/O circuits.

All of our products are compatible with all versions of Xilinx software, including the free WebPack software available from Xilinx.

Our system boards ship with a power supply and a programming cable, so designs can be implemented immediately without the need for any other components.
General Features

- Video via XSGA connector
- 10/100 Ethernet PHY + Connector
- Audio via AC97 codec and standard connectors
- Buttons, Switches, and LEDs
- RS-232
- Keyboard and mouse • 2 PS-2 Ports
Designed with Education in Mind

- Compact Flash card interface for individual project back-up or IBM Miicrodrives with upto 8Gbit capacity
- I/O under and over voltage protection
- Support for supply current monitoring
- USB port for FPGA Configuration using standard USB cable
- Self-test / configuration Flash memory
Memory Hierarchy

Virtex-II Pro XC2VP30 FPGA
- 2448 Kbits of BRAM
- 30,816 Logic Cells (Distributed RAM)

- Expandable memory up to 2 Gigabytes
- DDR SDRAM DIMM Slot

- Compact Flash card interface for individual project back-up or IBM Miicrodrives with up to 8Gbiyte capacity

- Non-volatile Platform Flash PROM for configuration storage
System Expansion

- High-speed connectors compatible with Digilent module boards
- High-speed Gigabit serial I/O
  - User Supplied SMA
- Additional I/O via user supplied four 60-pin headers
- Low-speed connectors compatible with Digilent peripheral boards
- High-speed Gigabit serial I/O
  - Serial ATA connectors
- Virtex-II Pro XC2VP30 FPGA
  - 4 of 8 Rocket I/O Tranceivers (MGTs)
  - 120 max of 556 User I/O
### Digilent System Expansion Modules

<table>
<thead>
<tr>
<th>Digital I/O 4</th>
<th>Digital Breadboard</th>
<th>1W Amplified Speaker</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital I/O 5</td>
<td>512K SRAM and Flash</td>
<td>1MHz Analog Acquisition</td>
</tr>
</tbody>
</table>

- Digilent Low cost, low speed plug-in modules to expand the curriculum
- High speed plug-in modules coming soon: video module in Jan 2005
- Visit www.digilentinc.com
Block Diagram

High-speed and low-speed I/O expansion connectors
Additional I/O via four user-supplied 60-pin headers
Three Serial ATA connectors
One 3.125 Gbps port via 4 user-supplied SMA connectors
10/100 Ethernet PHY
RS232
PS-2 (x2)
SVGA
Buttons (5), LEDs (4), switches (4)

DDR SDRAM DIMM
AC97 Audio CODEC & Stereo AMP
Compact Flash Configuration
USB Configuration
Platform Flash Configuration
External Power
Internal Power Supplies 3.3V, 2.5V, and 1.5V
100 MHz system clock
75 MHz SATA clock
2 user supplied clocks

Platform Flash Configuration

Internal Power Supplies

External Power

100 MHz system clock
75 MHz SATA clock
2 user supplied clocks

2VP30

Georgia Tech
http://www.xilinx.com/univ/

Xilinx University Program

General Information
- XUP Overview & Getting Started
- Xilinx Student Edition Software
- Xilinx University User Group
- Xilinx Design Series Textbooks

For XUP Members (Sign-up for access)
- Products & Pricing
- Professor Workshops
- Presentation Materials and Lab Files
- Course Examples, Research, Books, etc.
- Donation Program

What's New

Professor Workshops
If you have thought about teaching an engineering course which utilizes Programmable Logic technology, then attending a Professors Workshops is the best way to get started. These workshops involve on-site presentation combined with hands-on lab exercises on the PC. Workshops are taught mainly by industry professionals.

- DSP Workshop at Univ. of New Mexico - Thursday & Friday, August 6th & 6th

The great news is that these WORKSHOPS ARE FREE! Seats are limited at each event and demand is typically quite high, we recommend that you sign up as soon as possible. Workshop presentation and instruction may be offered in local language when appropriate and qualified instructor is available. Please see workshop schedule for more details.
Conclusions

- Programmable FPGA platforms are at the forefront of electronic systems design
- Simple entry point is to treat system on chip as shrunken version of system on board
- Opportunities for innovative use of (programmable) functional IP units, memories and (configurable) networks on chip
- Alternatives require not just new tools and methodologies, but also new thinking