### Sequence Pair Representation

- Initial SP:  $SP_1 = (17452638, 84725361)$ 
  - Dimensions: (2,4), (1,3), (3,3), (3,5), (3,2), (5,3), (1,2), (2,4)
  - Based on SP<sub>1</sub> we build the following table:

module	right-of	left-of	above	below
1	Ø	Ø	Ø	$\{2, 3, 4, 5, 6, 7, 8\}$
2	$\{3, 6\}$	$\{4, 7\}$	$\{1, 5\}$	$\{8\}$
3	Ø	$\{2, 4, 5, 7\}$	$\{1, 6\}$	$\{8\}$
4	$\{2, 3, 5, 6\}$	Ø	$\{1, 7\}$	$\{8\}$
5	$\{3, 6\}$	$\{4, 7\}$	$\{1\}$	$\{2, 8\}$
6	Ø	$\{2, 4, 5, 7\}$	$\{1\}$	$\{3,8\}$
7	$\{2, 3, 5, 6\}$	Ø	$\{1\}$	$\{4, 8\}$
8	Ø	Ø	$\{1, 2, 3, 4, 5, 6, 7\}$	Ø



# Constraint Graphs

- Horizontal constraint graph (HCG)
  - Before and after removing transitive edges





### Constraint Graphs (cont)

Vertical constraint graph (VCG)





### Computing Chip Width and Height

- Longest source-sink path length in:
  - HCG = chip width, VCG = chip height
  - Node weight = module width/height



### **Computing Module Location**

- Use longest source-module path length in HCG/VCG
  - Lower-left corner location = source to module <u>input</u> path length





Sequence Pair Method (5/13)

### Final Floorplan

### • Dimension: $11 \times 15$





# Move I

### ■ Swap 1 and 3 in positive sequence of SP<sub>1</sub>

- $SP_1 = (\underline{1}74526\underline{3}8, 84725361)$
- $SP_2 = (\underline{3}74526\underline{1}8, 84725361)$

module	right-of	left-of	above	below
1	Ø	$\{2, 3, 4, 5, 6, 7\}$	Ø	{8}
2	$\{1, 6\}$	$\{4, 7\}$	$\{3,5\}$	$\{8\}$
3	$\{1, 6\}$	Ø	Ø	$\{2, 4, 5, 7, 8\}$
4	$\{1, 2, 5, 6\}$	Ø	$\{3, 7\}$	$\{8\}$
5	$\{1, 6\}$	$\{4, 7\}$	$\{3\}$	$\{2, 8\}$
6	$\{1\}$	$\{2, 3, 4, 5, 7\}$	Ø	$\{8\}$
7	$\{1, 2, 5, 6\}$	Ø	$\{3\}$	$\{4, 8\}$
8	Ø	Ø	$\{1, 2, 3, 4, 5, 6, 7\}$	Ø









Practical Problems in VLSI Physical Design

Sequence Pair Method (8/13)

## Constructing Floorplan

#### • Dimension: $13 \times 14$

module	HCV	VCG
1	11	4
2	3	4
3	0	11
4	0	4
5	3	7
6	6	4
7	0	9
8	0	0





# Move II

### ■ Swap 4 and 6 in both sequences of SP<sub>2</sub>

- $SP_2 = (37\underline{4}52\underline{6}18, 8\underline{4}7253\underline{6}1)$
- $SP_3 = (37\underline{6}52\underline{4}18, 8\underline{6}7253\underline{4}1)$

module	right-of	left-of	above	below
1	Ø	$\{2, 3, 4, 5, 6, 7\}$	Ø	{8}
2	$\{1, 4\}$	$\{6,7\}$	$\{3,5\}$	$\{8\}$
3	$\{1, 4\}$	Ø	Ø	$\{2, 5, 6, 7, 8\}$
4	$\{1\}$	$\{2, 3, 5, 6, 7\}$	Ø	$\{8\}$
5	$\{1, 4\}$	$\{6,7\}$	$\{3\}$	$\{2, 8\}$
6	$\{1, 2, 4, 5\}$	Ø	$\{3, 7\}$	$\{8\}$
7	$\{1, 2, 4, 5\}$	Ø	$\{3\}$	$\{6, 8\}$
8	Ø	Ø	$\{1, 2, 3, 4, 5, 6, 7\}$	Ø









Practical Problems in VLSI Physical Design

Sequence Pair Method (11/13)

## Constructing Floorplan

#### • Dimension: $13 \times 12$

module	HCV	VCG
1	11	4
2	3	4
3	0	11
4	0	4
5	3	7
6	6	4
7	0	9
8	0	0





# Summary

- Impact of the moves:
  - Floorplan dimension changes from  $11 \times 15$  to  $13 \times 14$  to  $13 \times 12$

