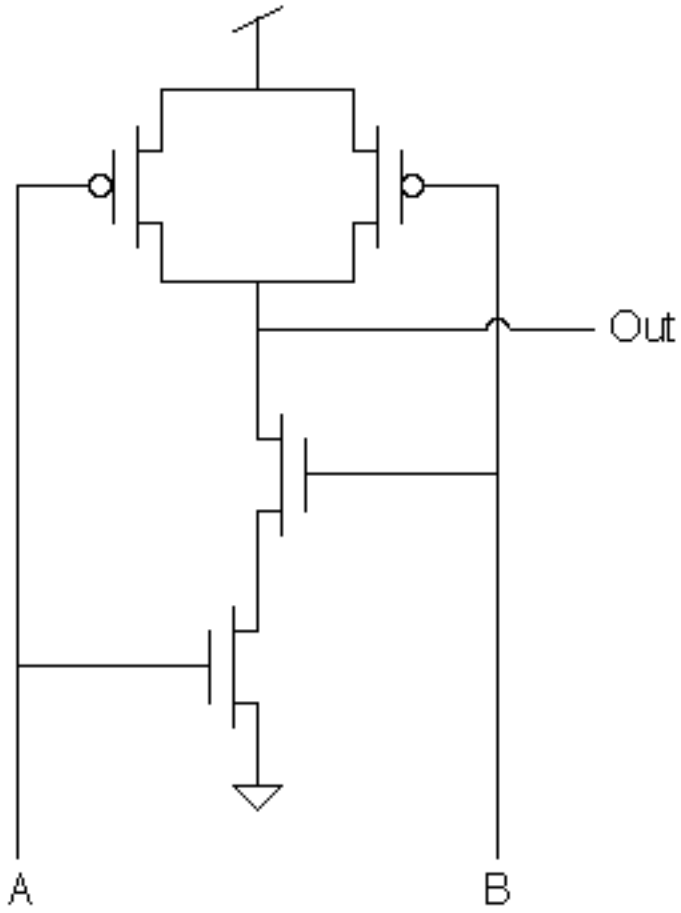
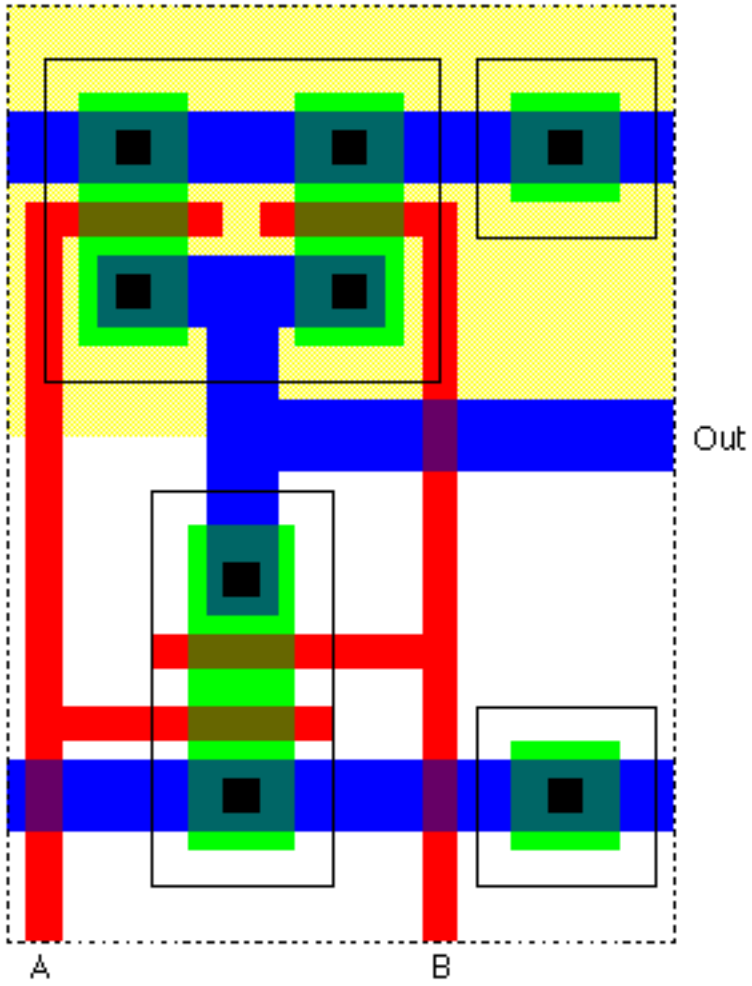
ECE 3060
VLSI and Advanced Digital Design

Lecture 5

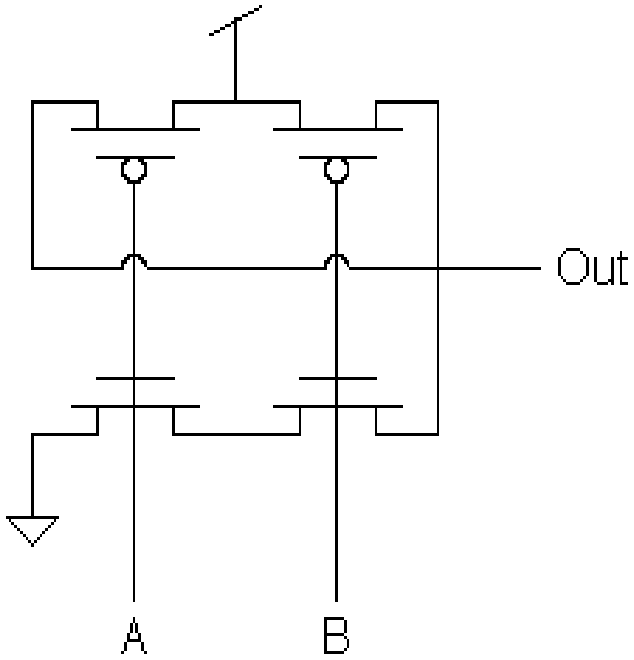
Complex Gates

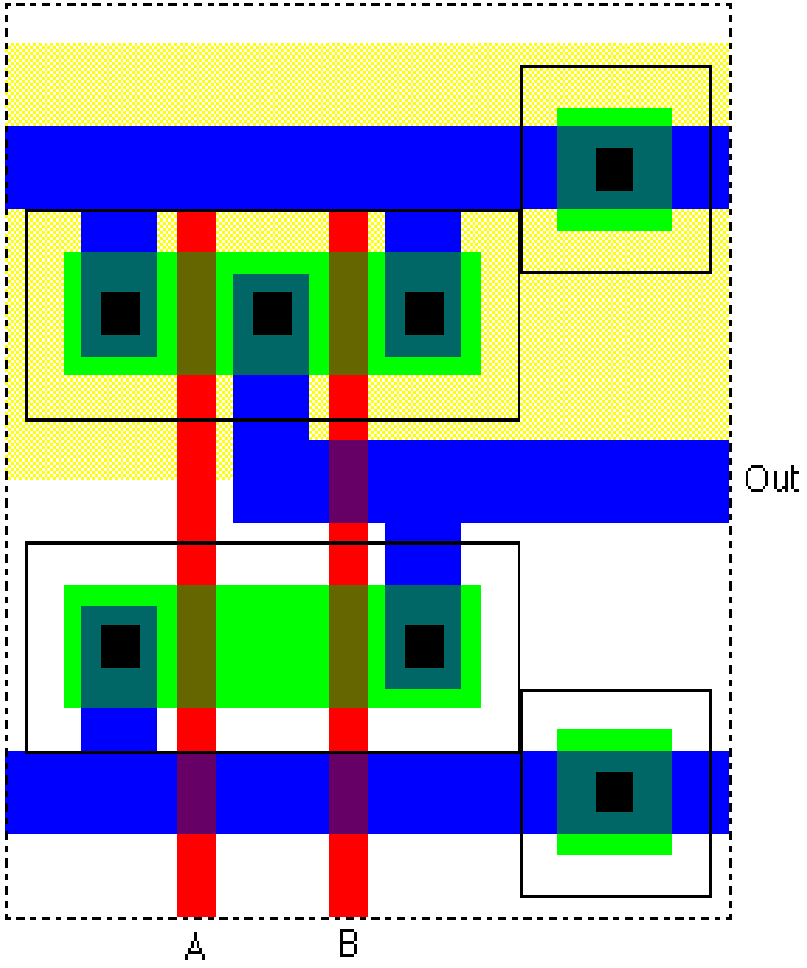
Example: NAND Gate (Vertical)





Example: NAND Gate (Horizontal)





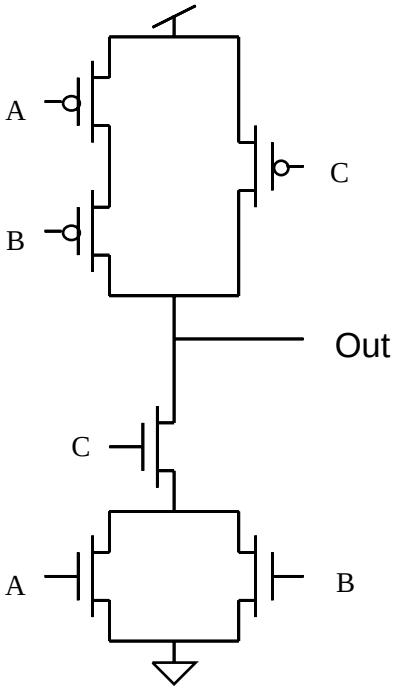
Other Gates

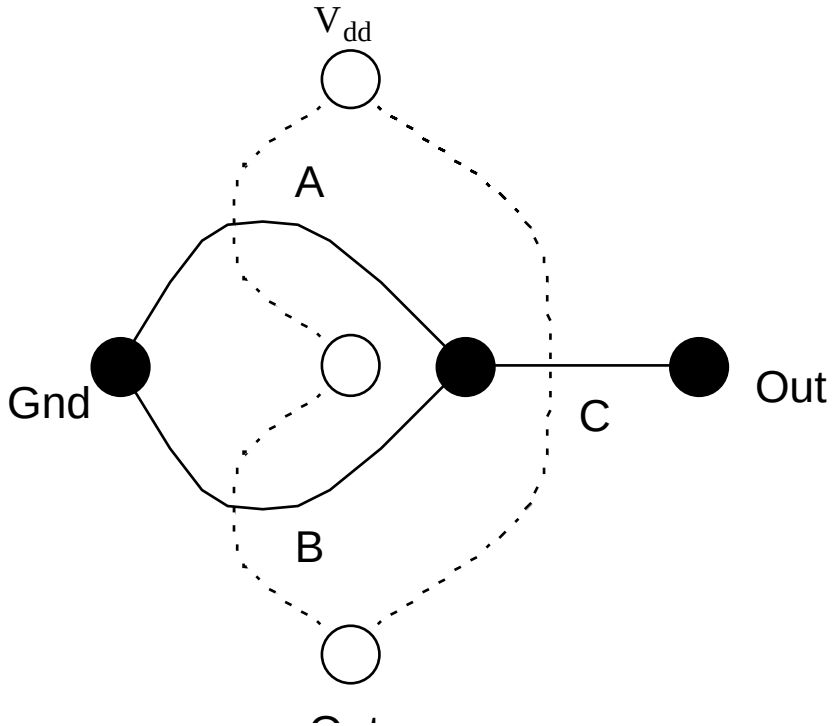
- And Or Invert (AOI)
- Or And Invert (OAI)
- XOR
- XNOR

Complex Gates

- **The gate "function" does not need to be primitive, or symmetric**
- **Any $f(x)$ may be implemented**
- **Algorithm:**
  1. put $f(x)$ in form with only AND, OR, and literals (use DeMorgans).
  2. compute $\overline{f}$ using generalized DeMorgan's Theorem
  3. construct complimentary networks using transistors in series for AND, and transistors in parallel for OR
- **Note: There are *many* correct networks due to commutivity**

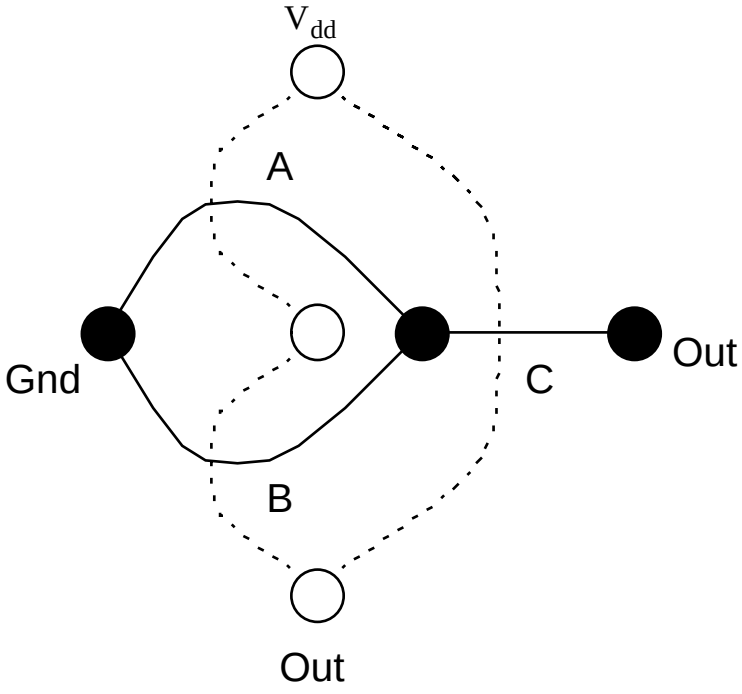
Euler Paths

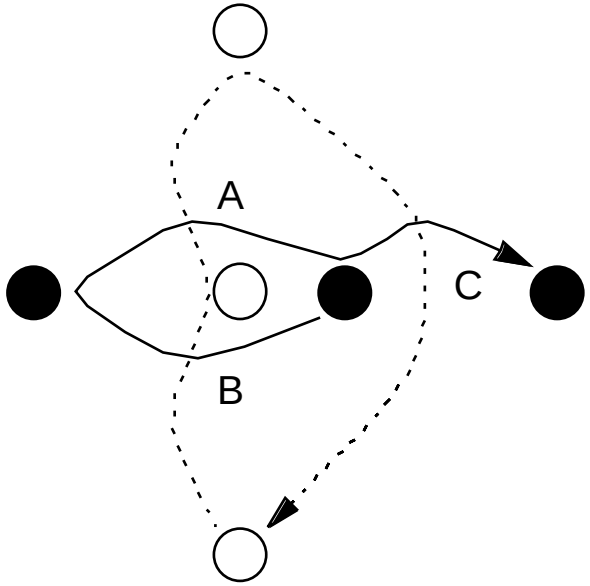




- **Mapping CMOS Circuits to Graphs**
  - **Circuit Nodes Map to Graph Vertices**
  - **Transistors Map to Graph Edges**
  - **Complementary Circuit Networks Map to Dual Graphs**

Euler Paths





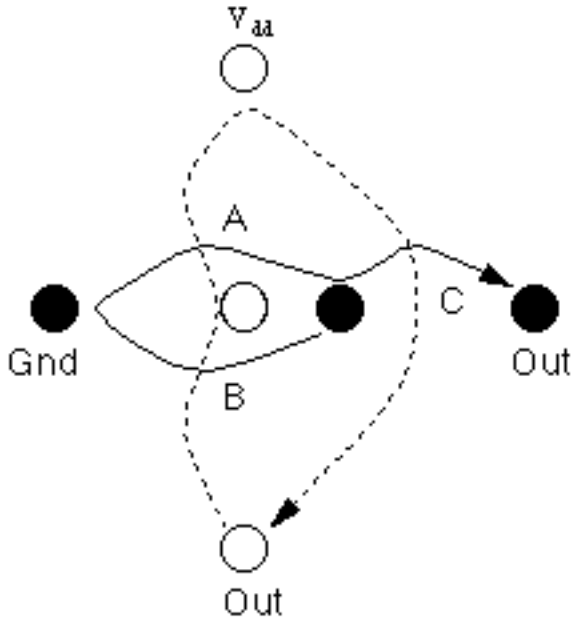
order = B, A, C

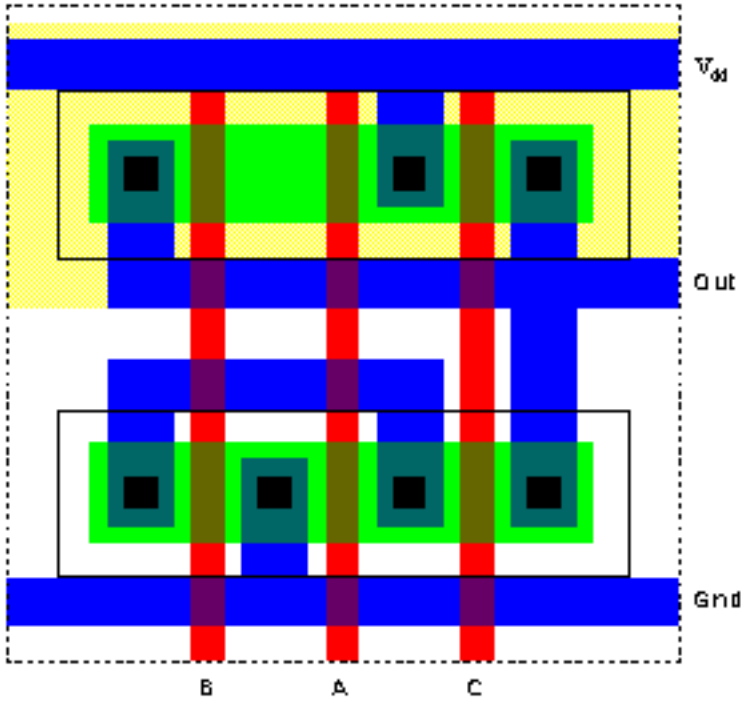
- **Finding Euler Paths**
  - **Find All Euler Paths**
  - **Find an n and a p Euler Path with Identical Labeling**
  - **If No Identical Labeling, Break the Path Minimally**

Describing an Euler Path

- While an ordered list of edges only suffice to denote an Euler path, a complete description is an ordered list of nodes and edges
- For example: Path = {V_{dd}, A, I_1, B, Out, C, V_{dd}}
- This form is useful for layout purposes

Euler Path to Layout





- **Map Euler Paths to CMOS Layout**
  - **Place Busses**
  - **Place Transistors**
  - **Complete Wiring**

Standard Cell Layout

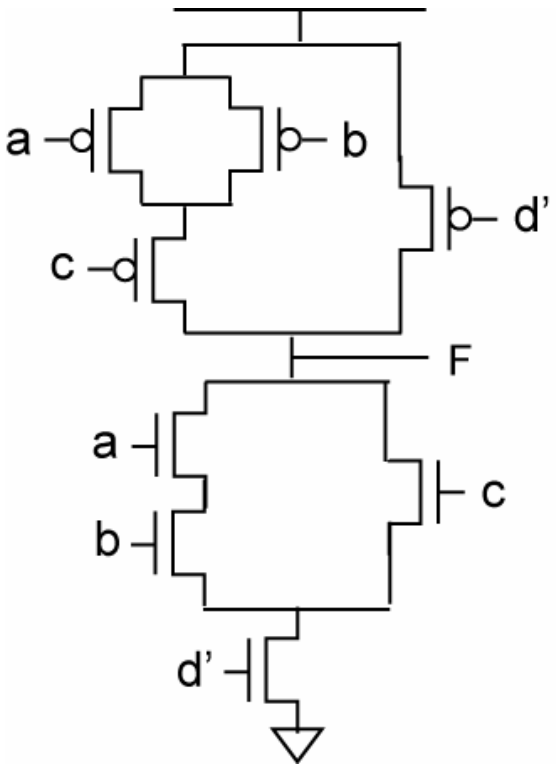
- In general, when laying out standard cells or other custom gate designs, there may not exist a Euler Path
  - e.g.,

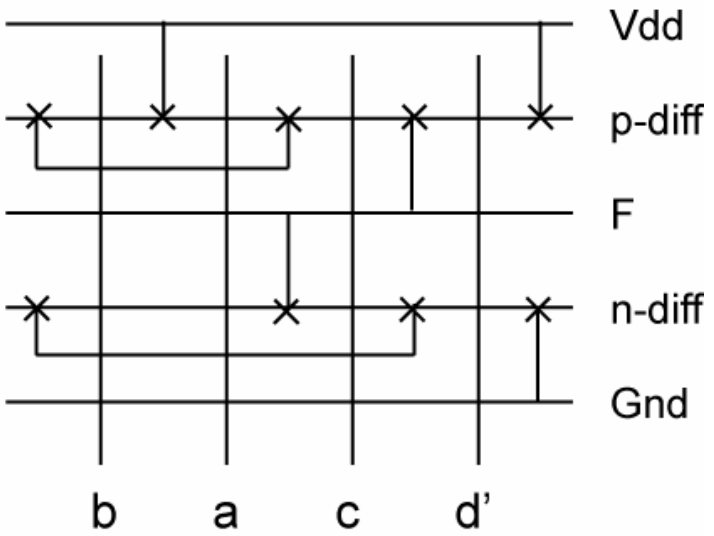
$$\overline{(AB + CD)E}$$

- Standard cells for a particular process (e.g., .35u HP CMOS) need not follow lamda spacing rules
- There are companies whose sole purpose is the creation and maintenance of standard cell libraries
- Custom layout is very time-intensive and laborious for large chips; therefore, custom layout is typically done only for critical paths
- Read Chapters 3, 4 and 7 of Wolf

Complex Gate vs Network of Gates

- Complex gate implementation of $F = \overline{ab + c} + d$





Complex Gate vs Network of Gates

- Network of NAND2/INV implementation