Tutorial I: Cadence Innovus

ECE6133: Physical Design Automation of VLSI Systems Georgia Institute of Technology Prof. Sung Kyu Lim

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I. Setup for Cadence Innovus

1. Copy the following files into your working directory.

- gscl45nm.lef
- gscl45nm.tlf
- gscl45nm.map
- test.sdc
- test.v

2. Type the following command to source the designated file. source /tools/software/cadence/innovus/cshrc.latest

A If you get the error:

bash: setenv: command not found...

You need to type *csh* in the terminal to switch to the C shell.

3. Run Cadence Innovus by typing 'innovus'. Do not use background command (= innovus &').

▲ If you get the warning ***WARN: (IMPSYT-1507): The display is invalid and will start in no window mode*, you need to reconnect through SSH using the command for trusted X11 forwarding: ssh -XY server_name

4. Cadence Innovus manual provided by Cadence can be found in the following directory. /tools/software/cadence/innovus/docs/20.1/innovusUG/innovusUG.pdf

II. Placement and Routing

1. Importing Your Design

A. Click File \rightarrow Import Design in menu bar

Netlist:		
Verilog		1
Files:	(2)	U
	Top Cell: Auto Assign 💿 By User:	
O OA		
Library:		-
Cell:		· · · · · ·
View:		
Technology/Physical Libraries	•	
• OA		
Reference Libraries:		
Abstract View Names:		
3 Layout View Names:		
C LEF Files		
Floorplan		
IO Assignment File:		E
Power		
Power Nets:		
Ground Nets:		
CPF File:		D
Analysis Configuration		
MMMC View Definition File:		D
	Create Analysis Configuration 5	

B. Click the button '1', click the open button in 'Netlist Files' window, expand the window by clicking ">>>", add your netlist file (test.v) by double-clicking, and close the 'Netlist Files' window.

	Netlist Files (on eceling	srvx.ece.gatech.edu)	×
Netlist File: test.v	click Add <<	Netlist Selection:	
Netlist Files:		/nethome/kchang63/temp/ece6133_proj	
		 gscl45nm.lef gscl45nm.map gscl45nm.tlf innovus.cmd innovus.log innovus.logv test.v 	
		Filters: Netlist Files (*.v*)	
	Clos	e	

C. Click the button '2' to make Innovus find the top cell automatically.

D. Click the button '3' which enables LEF Files and click '4' to open 'LEF Files' window, expand the window by clicking ">>", add 'gscl45nm.lef' by double-clicking, and close the 'LEF Files' window.

	LEF Files (on ecelinsrvx.ece.gatech.edu)
LEF File: gscl45nm.lef LEF Files:	Add << LEF Selection:
gscl45nm.lef	iii gscl45nm.lef iii gscl45nm.map iii gscl45nm.tif iii innovus.cmd iii innovus.log iii innovus.logv iii test.vi
	Filters: LEF Files (*.lef)
	Close

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nalysis View List	MMMC Objects	Wizard Help
Analysis Views (d) Setup Analysis Views (e) Hold Analysis Views (f)	Library Sets (a) RC Corners OP Conds Delay Corners (b) Constraint Modes (c)	 This wizard will assist you in specifying the necessary information to configure the system for RC extraction, delay calculation, and timing analysis. It you have all the necessary data available, it is recommended that you configure the system as completely as possible for all steps of the implementation flow - through signoff. If not, you can always update the configuration, if necessary, as you proceed through the flow. If you are comfortable using the MMMC Browser, you can use the Wizard Off button to remove the help dialog, and proceed at your own pace. For additional assistance with design import, press the Next button
		Prev

E. Click the button '5' which opens MMMC Browser. More steps follow:

 a) Double click (a) "Library Sets" (not '+' button) which opens "Add Library Set" window. Type "gscl45nm_ls" on Name field, click Add button in "Timing Library Files" tab which opens "Timing Library Files" window.

Name: gscl45nm_ls Timing Library Files		SI Library Files	
	Add Delete		Add Delete
<u>o</u> k	Apply		Help

b) In the "Timing Library Files" window, expand the window by clicking ">>", change Filters to "All Files (*)", and double-clickgscl45nm.tlf, and close the window.

ing Library Selection: /nethome/kchang63/temp/ece6133_proj 💽 💽
/nethome/kchang63/temp/ece6133 proj 📃 🛜
methomemangositempreceorss_proj
gscl45nm.lef gscl45nm.map gscl45nm.tlf innovus.log innovus.logv test.v
rs: All Files (*)

c) Close the "Add Library Set" Window by clicking "OK".

me: gscl45nm_ls		SI Library Files	
gscl45nm.tlf	_		
	Add Delete		Add Delete
			Contract

d) In MMMC Browser, double click (b) "Delay Corners" which opens "Add Delay Corner" window. Type "gscl45nm_dc" in Name field, and select gscl45nm_ls for Library Set in Attribute tab. Then Close the window with clicking "OK".

wer Domain List		Туре
fault		On Chip Variation Single/BcWc
		Attributes
		RC Corner:
		Library Set: gscl45nm_ls
		OpCond Lib:
		OpCond:
		IrDrop File:
		Early
	Add	Library Set
	Delete	OpCond Lib:
		OpCond
		IrDrop File:
		Late
		Library Set:
		OpCond Lib:
		OpCond:
		IrDrop File:

e) In MMMC Browser, double click (c) "Constraint Modes" which opens "Add Constraint Mode" window. Type "test_cm" on Name field, click Add button in "SDC Constraint Files" tab which opens "Timing Library Files" window.

SDC Constraint Files	_	ILM Constraint Files	_
	Add		Add

f) In the "SDC Constraint Files" window, expand the window by clicking ">>", and double-click test.sdc, and close the window.

SDC Co	nstraint Files (on ecelinsrvx.ece.gatech.edu)
DC Constraint File: test.sdc SDC Constraint Files:	Add Constraint Selection:
test.sdc	<pre>/nethome/kchang63/temp/ece6133_proj gscl45nm.lef gscl45nm.thf gscl45nm.thf innovus.cmd innovus.log innovus.logv test.sdc test.v</pre>
	Delete Close

	ILM Constraint F	iles
-		
Add		Add
Delete		Delete
	Add Delete	Add

g) In MMMC Browser, double-click (d) "Analysis Views" which opens "Add Analysis View" window. Type "test_av" in the Name field and select (or confirm) gsc45nm_dc in Delay Corner field. Click 'OK' to close the window.

🖬 Add Analysis	View (on ece 💶 🗆 🗙
Name:	test_av
Constraint Mode:	test_cm 🔽
Delay Corner:	gscl45nm_dc
	gscl45nm_dc

h) In MMMC Browser, double-click (e) "Setup Analysis Views" which opens "Add Setup Analysis View" window. Select (or confirm) "test_av" in Analysis View field. Click 'OK' to close the window.

📕 Add Setup Analysis View	4 <u>88</u> 5		x
Analysis View:test_av			-
OK Apply Close	E	<u>l</u> elp	

Do the same for (f) "Hold Analysis Views".

Add Hole	d Analysis View (+	-		×
Analysis View:	test_av			-
ОК	Apply Close	Ŀ	<u>l</u> elp	

i) The resulting MMMC Browser should look like the figure below. Click save & Close and save it as "Default.view".

È-Analysis Views È-test_av È-Setup Analysis Views È-test_av □ Hold Analysis Views	⊡ Library Sets ⊡ gscl45nm_ls ⊞ RC Corners	
È⊢ test_av	⊕ OP Conds ⊖ Delay Corners ⊡ gscl45nm_dc ⊖ Constraint Modes ⊕ test_cm	This wizard will assist you in specifying the necessary information to configure the system for RC extraction, delay calculation, and timing analysis. It you have all the necessary data available, it is recommended that you configure the system as completely as possible for all steps of the implementation flow - through signoff. If not, you can always update the configuration, if necessary, as you proceed through the flow. If you are comfortable using the MMMC Browser, you can use the Wizard Off button to remove the help dialog, and proceed at your own pace. For additional assistance with design import, press the Next button
		Prev

j) Your 'Design Import' window should look like the following.

Netlist:		
🥑 Verilog		
Files:	test.v	
	Top Cell: Auto Assign 🔾 By User: Ictest	
O OA		
Library:		
Cell:		1
View		1
Technology/Physical Librar	ies:	
O OA		
Reference Libraries:		
Abstract View Names		
Layout View Names:		
LEF Files	gscl45nm.lef	
Floorplan		
IO Assignment File:		B
Power		
Power Nets:		
Ground Nets:		
CPF File:		6
Analysis Configuration		
MMMC View Definition File	Default.view	6
	Create Analysis Configuration	

k) Click 'OK' to import your design. Look at your command shell window. Innovus shows various information while it imports the design. The main window of Innovus will show you rows, where standard cells will be placed during placement.

2. Setting Up Layout Area

In this step, we will set up layout area. We will not do floorplanning.

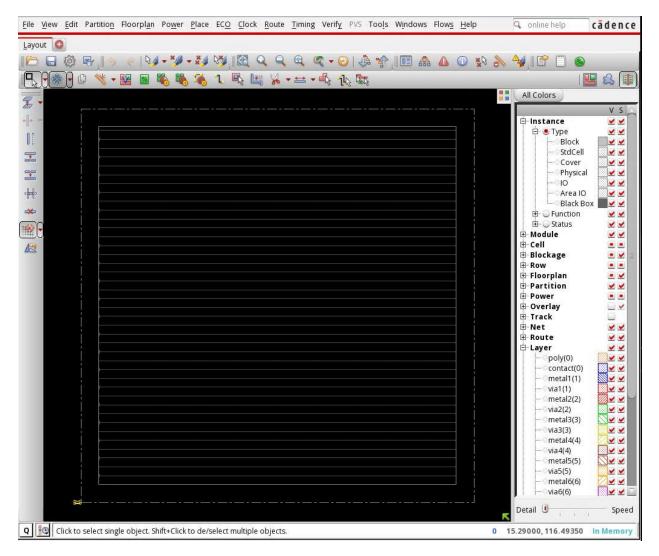
A. Choose 'Floorplan' and then 'Specify Floorplan ...' in the menu bar

B. In 'Basic' tab, you can specify core size by (1) AR (Aspect Ratio) or (2) Dimension. 'Core' is the region that cells are placed.

C. Choose 'Dimension' under 'Core Size by' and set width and height to be 100. (100 by 100 is actually too large for this design. You will be asked to change the width and height later.)

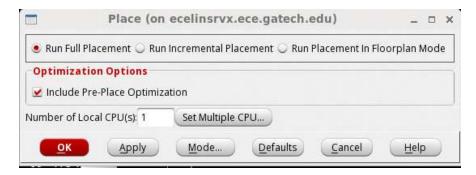
D. Choose 'Core to IO Boundary' and set 'Core to Left', 'Core to Top', 'Core to Right' and 'Core to Bottom' to 5

E. Click 'OK' to finish and see the modified floorplan outline in the main window. It should look like the following.



3. Performing Placement

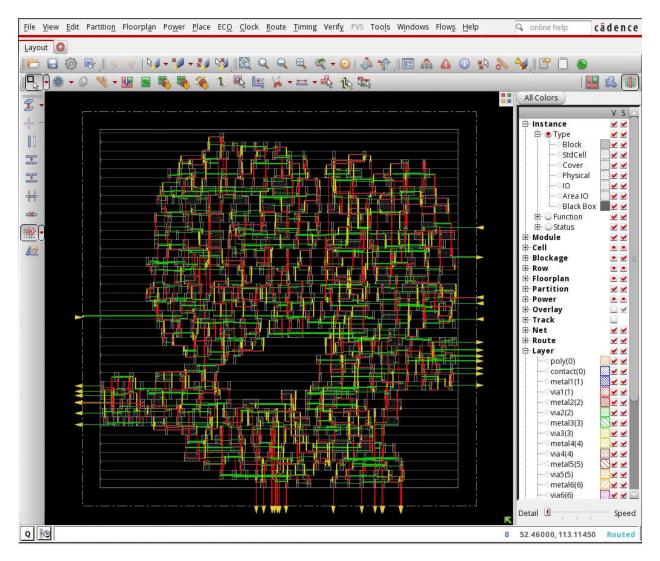
A. Choose 'Place' -> 'Place Standard Cell...' then you will see the following window.



B. Click 'Mode...', click "Set Defaults", and click "OK".

CTS	Placement RefinePlace				
EarlyGlobalRoute EndCap Filler NanoRoute OasisOut	 Congestion Effort Low Medium High Auto Run Placement In FloorPlan Mode Run Timing Driven Placement 				
Optimization Placement	✓ Rah Hinning Diven Flacement ✓ Enable Module Plan				
ScanReorder	Enable Module Plan Enable Clock Gating Awareness				
StreamOut	Enable Power Driven				
TieHiLo	 Ignore Scan Connections Reorder Scan Connection Ignore Spare Cell Connections Place IO Pins Hierarchy Aware Spare Cell Placement Specify Maximum Density Layers Checked For Pin Access 				
	Specify Maximum Routing Layer 1				

C. In Place Window, click 'OK" to perform placement. Innovus will do placement as well as trial-routing (It is not actual routing)



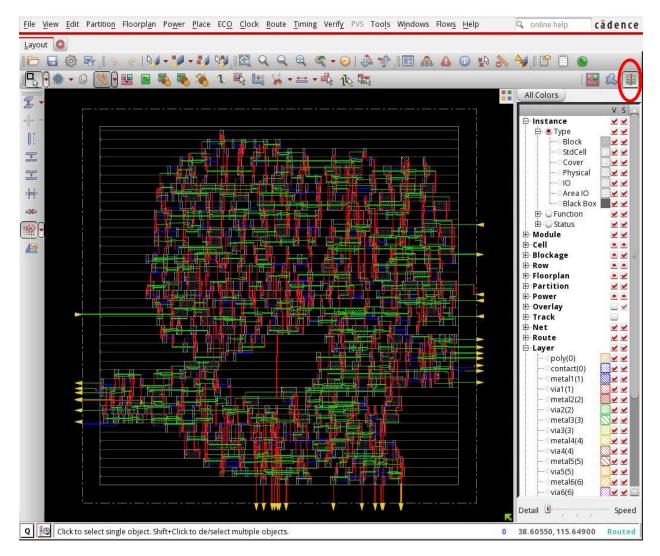
D. To see the core utilization, click '%' button in the toolbar and drag and make a rectangle containing the core region. The utilization will be shown in your command shell window. It will be about 22.1% in this example.

4. Performing Routing

A. Choose 'Route' -> 'Nanoroute' -> 'Route...' then you will see the following window.

Routing Phase	
⊻ Global Route	
🗹 Detail Route End Ite	ration 1
Post Route Optimization	n 🔲 Optimize Via 🛄 Optimize Wire
Concurrent Routing F	eatures
🗹 Fix Antenna	Insert Diodes Diode Cell Name
Timing Driven	Congestion Timing Effort 5 S.M.A.R.T.
SI Driven	
🔲 Litho Driven	
🔲 Post Route Litho Rep	bair
Routing Control	
Selected Nets Only	Bottom Layer 1 Top Layer 10
ECO Route	
💷 Area Route	Area Select Area and Route
Job Control	
🗹 Auto Stop	
Number	r of Local CPU(s): 1
Number of CPU(s) per R	lemote Machine: 1
Number of Ren	note Machine(s): 0
Set Multiple CPU	

B. Click 'OK' to do routing with default settings. Click 'Physical view' button (highlighted with red circle in the following window) and see the routing result. It should look like the following.

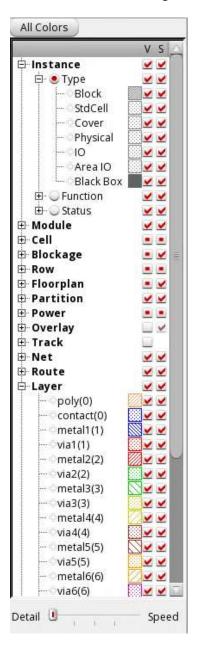


C. See your command shell window. It shows the routing information such as total wirelength, total wirelength in each metal layer, the number of vias, the number of DRC violations, and so on.

D. How to capture screenshots: Choose 'Tools' -> 'Screen Capture' -> "Write To GIF File..."

5. How to View Specific Metal Layers and Vias

On the right side of the screen, scroll down and see the following items.



You can turn on and off the visibilities of metal layers and vias. Turn on and off visibilities and see if it works well. You will need this to capture specific metal layers later.

III. GDSII File Generation

After finishing up to routing step, you have to save your design to make a final layout which includes layouts of standard cells. This step is done by Cadence Virtuoso, thus you have to save your design and load it in Virtuoso. We will use gdsii format for this.

1. GDS Export

Choose 'File' -> 'Save' -> 'GDS/OASIS...' then you will see the following window.

Output Forma	t 🕔	9 GDSII/Stream	O OASIS			
Output File						0
Map File str	eamO	ut.map				
Library Name	Desig	nLib				
🔲 Structure Na	me	ictest				
📃 Attach Insta	nce Na	me to Attribute N	umber			
🔲 Attach Net N	lame t	o Attribute Numb	er			
🗌 Merge Files			10	🛄 Ur	niquify Cell N	lames
🗌 Stripes 🗻						
📃 Write Die Ar	ea as l	Boundary				
📃 Write abstra	ict info	rmation for LEF N	lacros			
Units 2000						
Mode ALL >	J					
<u>о</u> к		Apply	Cancel)	Help	

2. Setting

Use the following setting:

- Output Format : GDSII/Stream
- Output File : type a file name for gdsii output file.
- Map File : choose 'gscl45nm.map'
- Library Name : test (for test.v), IC1 (for IC1.v), IC2 (for IC2.v), IC3 (for IC3.v)
- GDS Structure Name : same as Library Name

The GDS Export window should look like the following.

Output Format 💿 GDSII/Stream 🔾 OASIS
Output File test.gds2
Map File input_files/gscl45nm.map
Library Name test
Structure Name test
Attach Instance Name to Attribute Number
Attach Net Name to Attribute Number
Merge Files Uniquify Cell Names
Write Die Area as Boundary
Write abstract information for LEF Macros
Units 2000 >
Mode ALL >
OK Apply Cancel Help

Click 'OK' to save your design.

IV. Exercise

Try these to enhance your understanding of Cadence Innovus. You don't need to submit the answers to these items.

- 1. Try the whole step with the same netlist file (test.v) and the modified core area (30x30). You don't need to turn off and on Innovus. Just start from '2.2 setting-up of layout area' step. After placement is done, check out your command shell window. You will see error messages because core area is too small.
- 2. Try the whole step with the same netlist file with the modified core area (N by N). At this time, try with various N values and find the minimum N which passes placement and routing without any error.
- "Specify Maximum Routing Layer" in placement step. In "Mode Setup" window (2.3.b in placement step), Set "Specify Maximum Routing Layer" as 2.

CTS Placement RefinePlace EarlyGlobalRout Congestion Effort Filler Congestion Effort Filler Congestion Effort NanoRoute NanoRoute OasisOut Run Placement In FloorPlan Mode Optimization Run Timing Driven Placement Placement Enable Module Plan ScanReorder Enable Clock Gating Awareness StreamOut Ignore Scan Connections IelHILO Ignore Scan Connections Ignore Spare Cell Connections Place IO Pins Hierarchy Aware Spare Cell Placement Hierarchy Aware Spare Cell Placement	List of Modes	Placement Mode	
EndCap Image: Congestion Effort Filler Image: Low Image: Medium Image: High Image: Auto NanoRoute Image: Run Placement In FloorPlan Mode OasisOut Image: Run Placement In FloorPlan Mode Optimization Image: Run Timing Driven Placement Placement Image: Run Timing Driven Placement ScanReorder Image: Runble Clock Gating Awareness StreamOut Image: Runble Power Driven TieHILO Image: Reorder Scan Connections Image: Reorder Scan Connections Image: Reorder Scan Connections Image: Reorder Scan Connections Image: Reorder Scan Connections Image: Place IO Pins Image: Place IO Pins	CTS	Placement RefinePlace	
	EndCap Filler NanoRoute OasisOut Optimization Placement ScanReorder StreamOut	 Low Medium High Auto Run Placement In FloorPlan Mode Run Timing Driven Placement Enable Module Plan Enable Clock Gating Awareness Enable Power Driven Ignore Scan Connections Reorder Scan Connection Ignore Spare Cell Connections Place IO Pins 	
Specify Maximum Density -1.0 Layers Checked For Pin Access 1 Select		and the second	Select
Specify Maximum Routing Layer 2		Specify Maximum Routing Layer	•
Set Defaults		Set Defaults	

After placement is done, open NanoRoute window and set 'Top Layer' in 'Routing Control' box. The value in 'Top Layer' box should be 2 which you specified during placement.

Routing Phase			
🗹 Global Route			
Detail Route End Ite	ration 1		
Post Route Optimization	🛛 🗌 Optimize Via 🔲 Optim	ize Wire	
Concurrent Routing Fe	atures		
🗹 Fix Antenna	Insert Diodes	Diode Cell Name	
Timing Driven	Effort 5	stion Timing	S.M.A.R.T.
SI Driven			
Litho Driven			
🔲 Post Route Litho Rep	air		
Routing Control			
Selected Nets Only	Bottom Layer 1	Top Layer 2	
ECO Route			
🔲 Area Route	Area	Sel	ect Area and Route
Job Control			
🗹 Auto Stop			
Number	of Local CPU(s): 1		
Number of CPU(s) per R	emote Machine: 1		
Number of Ren	note Machine(s): 0		
Set Multiple CPU			

Run nanoroute and see the number of metal layers used in routing in your command shell window.