Tutorial I: Cadence Innovus

ECE6133: Physical Design Automation of VLSI Systems
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I. Setup for Cadence Innovus

1. Copy the following files into your working directory.
    - gscl45nm.lef
    - gscl45nm.tlf
    - gscl45nm.map
    - test.sdc
    - test.v

2. Type the following command to source the designated file.
    source /tools/software/cadence/innovus/cshrc.latest

⚠ If you get the error:

```
bash: setenv: command not found...
```

You need to type ***csh*** in the terminal to switch to the C shell.

3. Run Cadence Innovus by typing 'innovus'. Do not use background command (= innovus &').

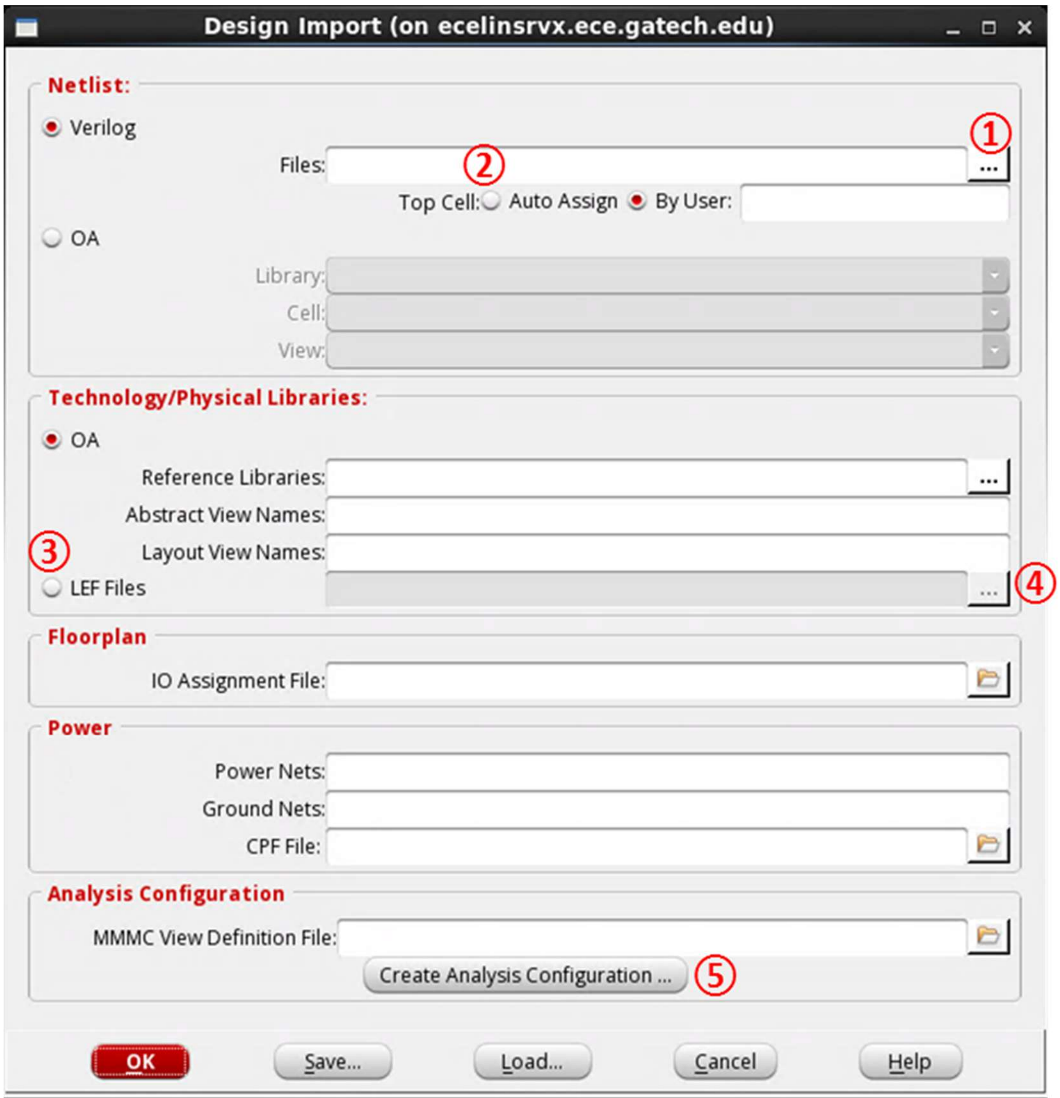
⚠ If you get the warning *****WARN: (IMPSYT-1507): The display is invalid and will start in no window mode***, you need to reconnect through SSH using the command for trusted X11 forwarding:
    ssh -XY server_name

4. Cadence Innovus manual provided by Cadence can be found in the following directory.
    /tools/software/cadence/innovus/docs/20.1/innovusUG/innovusUG.pdf

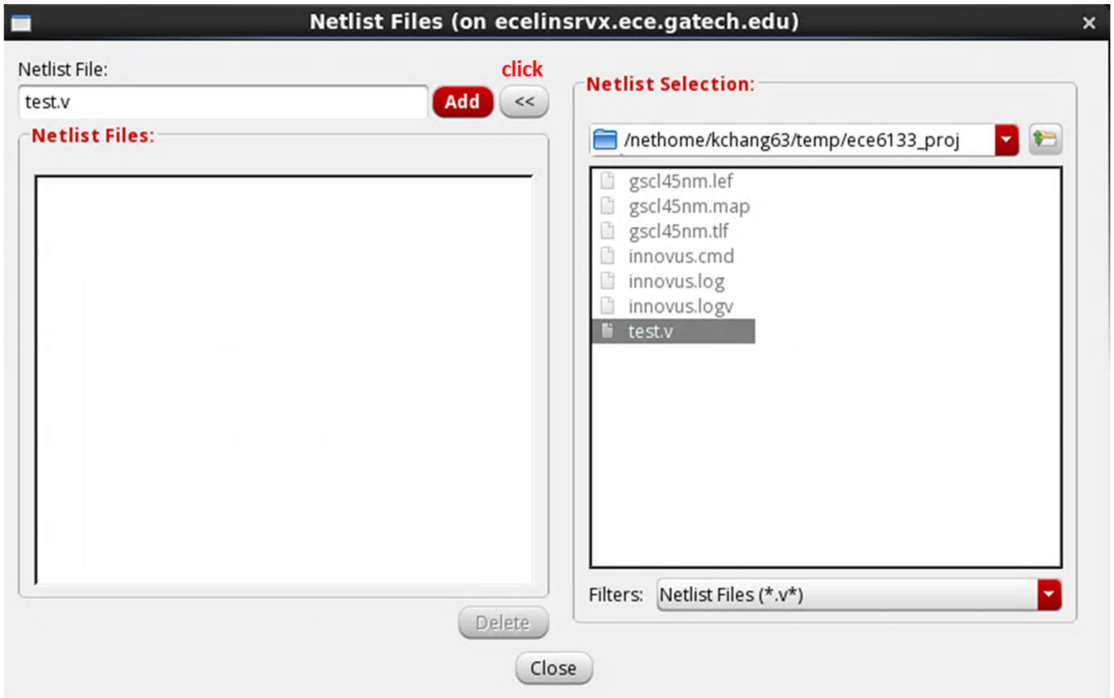
II. Placement and Routing

1. Importing Your Design

A. Click File → Import Design in menu bar



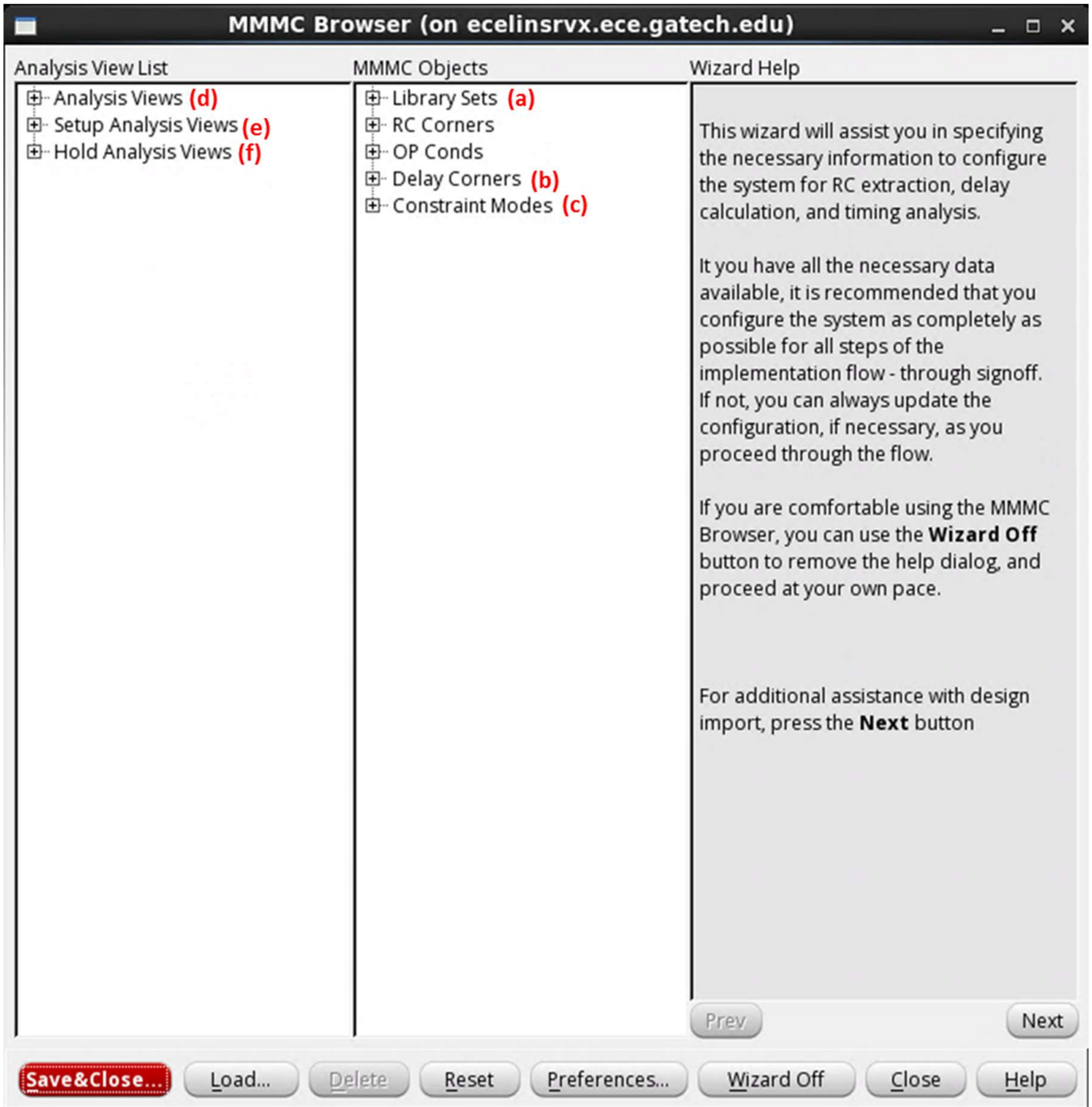
B. Click the button '1', click the open button in 'Netlist Files' window, expand the window by clicking “>>”, add your netlist file (test.v) by double-clicking, and close the 'Netlist Files' window.



C. Click the button '2' to make Innovus find the top cell automatically.

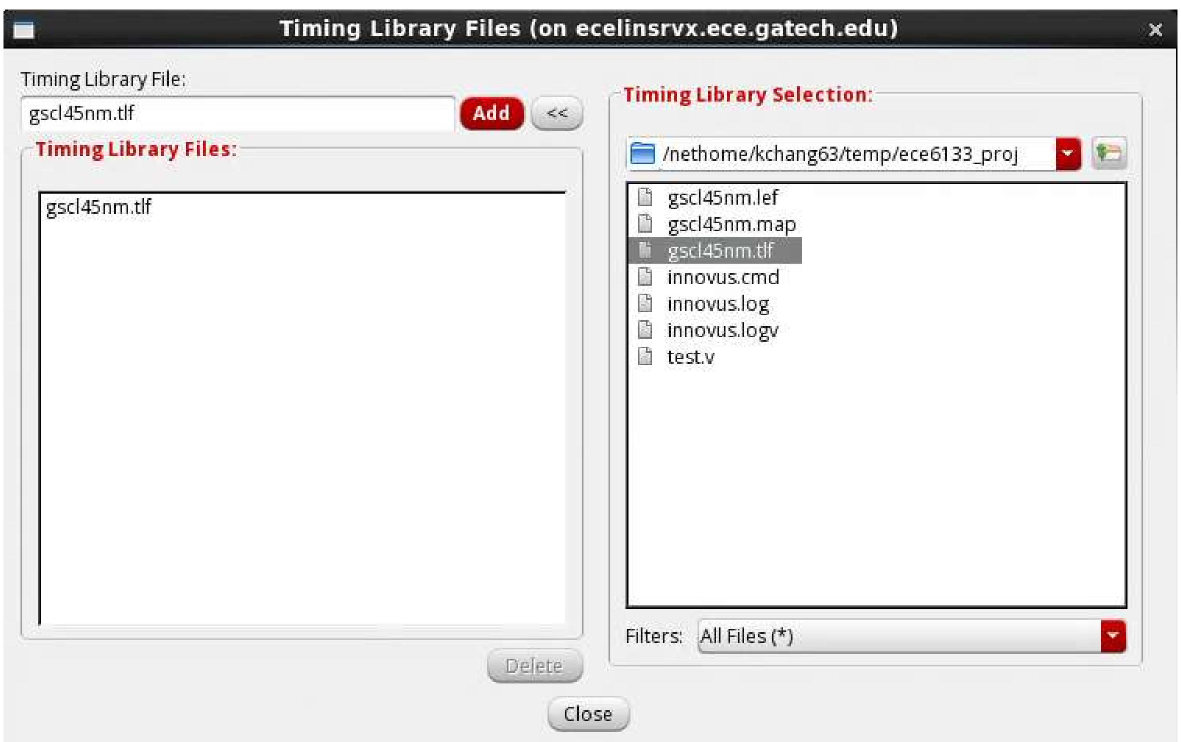
D. Click the button '3' which enables LEF Files and click ‘4’ to open 'LEF Files' window, expand the window by clicking “>>”, add 'gscl45nm.lef' by double-clicking, and close the 'LEF Files' window.

E. Click the button '5' which opens MMMC Browser. More steps follow:



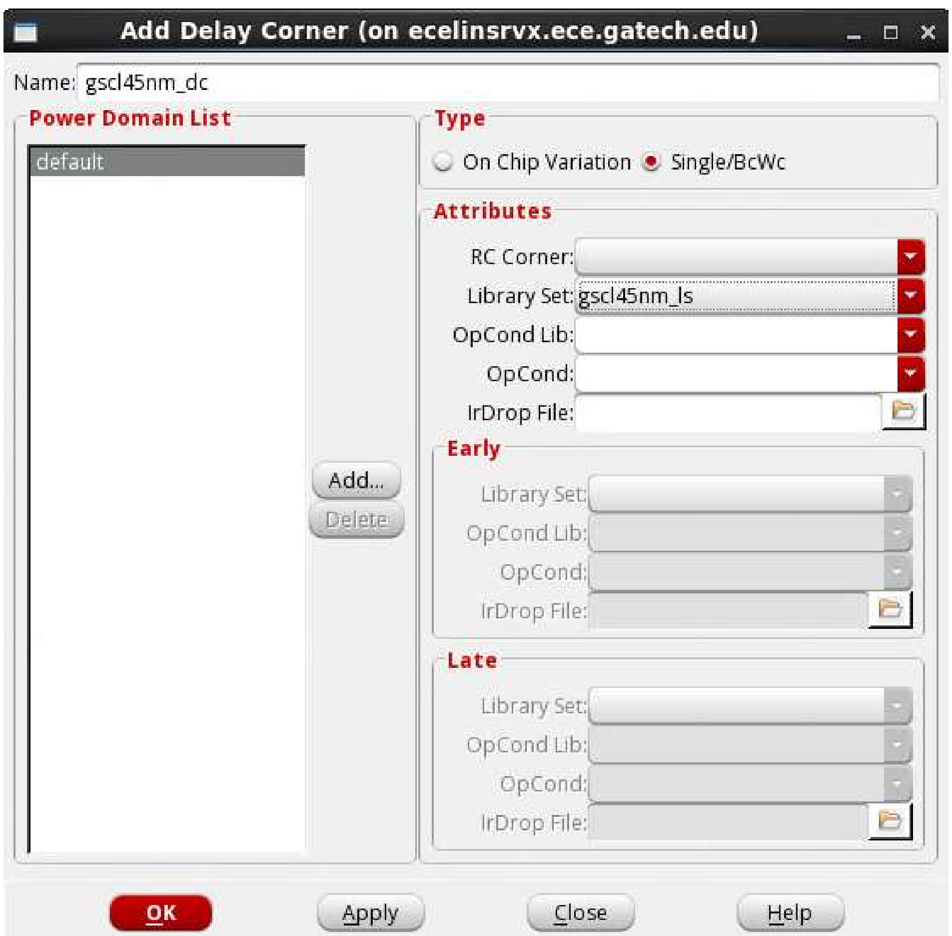
a) Double click (a) “Library Sets” (not ‘+’ button) which opens “Add Library Set” window. Type “gscl45nm_ls” on Name field, click Add button in “Timing Library Files” tab which opens “Timing Library Files” window.

b) In the “Timing Library Files” window, expand the window by clicking “>>”, change Filters to “All Files (*)”, and double-clickgscl45nm.tlf, and close the window.

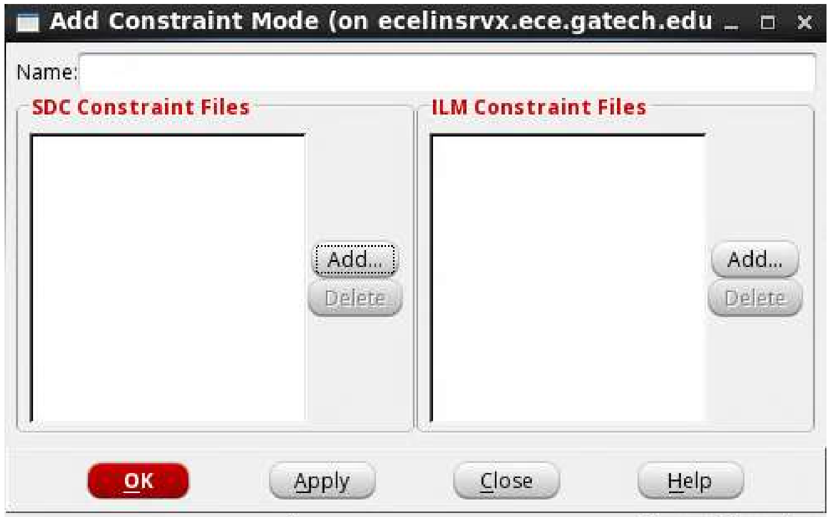


c) Close the “Add Library Set” Window by clicking “OK”.

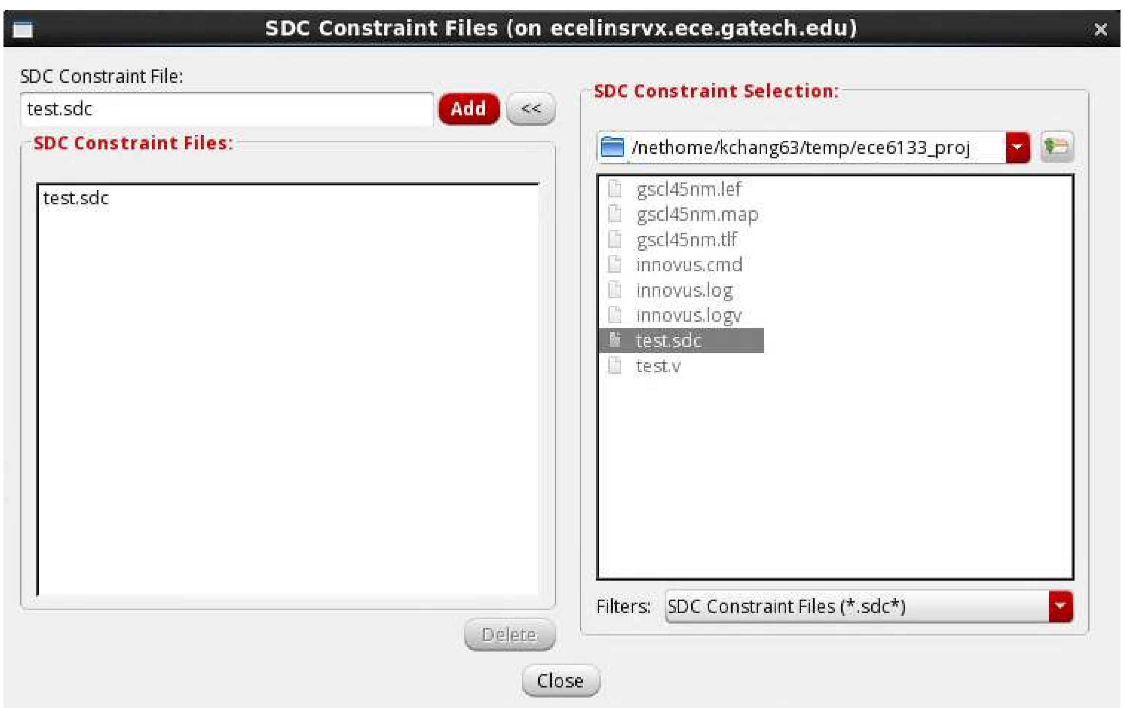
d) In MMMC Browser, double click (b) “Delay Corners” which opens “Add Delay Corner” window. Type “gscl45nm_dc” in Name field, and select gscl45nm_ls for Library Set in Attribute tab. Then Close the window with clicking “OK”.

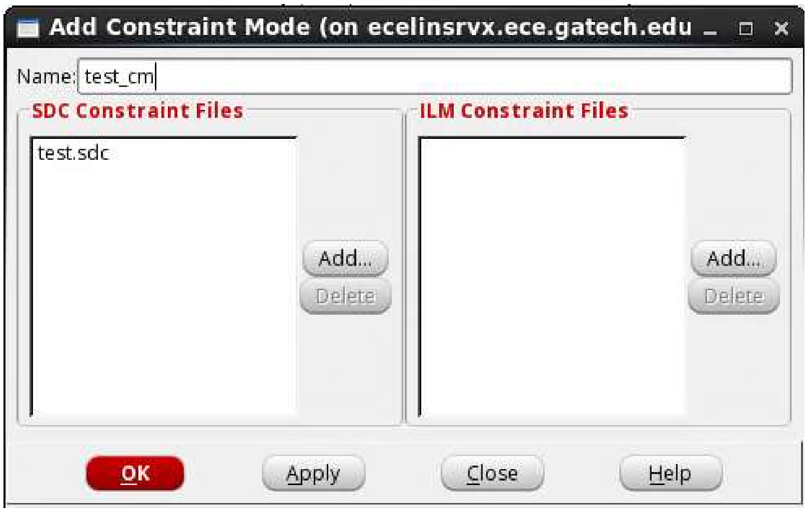


e) In MMMC Browser, double click (c) "Constraint Modes" which opens "Add Constraint Mode" window. Type "test_cm" on Name field, click Add button in "SDC Constraint Files" tab which opens "Timing Library Files" window.

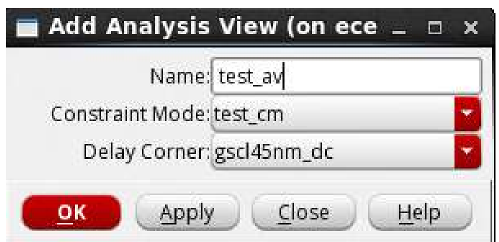


f) In the "SDC Constraint Files" window, expand the window by clicking ">>", and double-click test.sdc, and close the window.



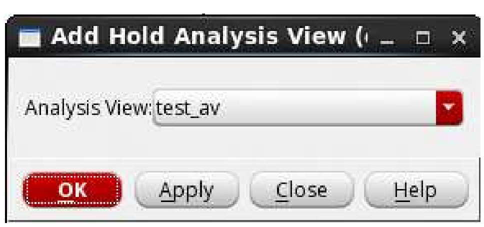


g) In MMMC Browser, double-click (d) “Analysis Views” which opens “Add Analysis View” window. Type “test_av” in the Name field and select (or confirm) gsc45nm_dc in Delay Corner field. Click ‘OK’ to close the window.

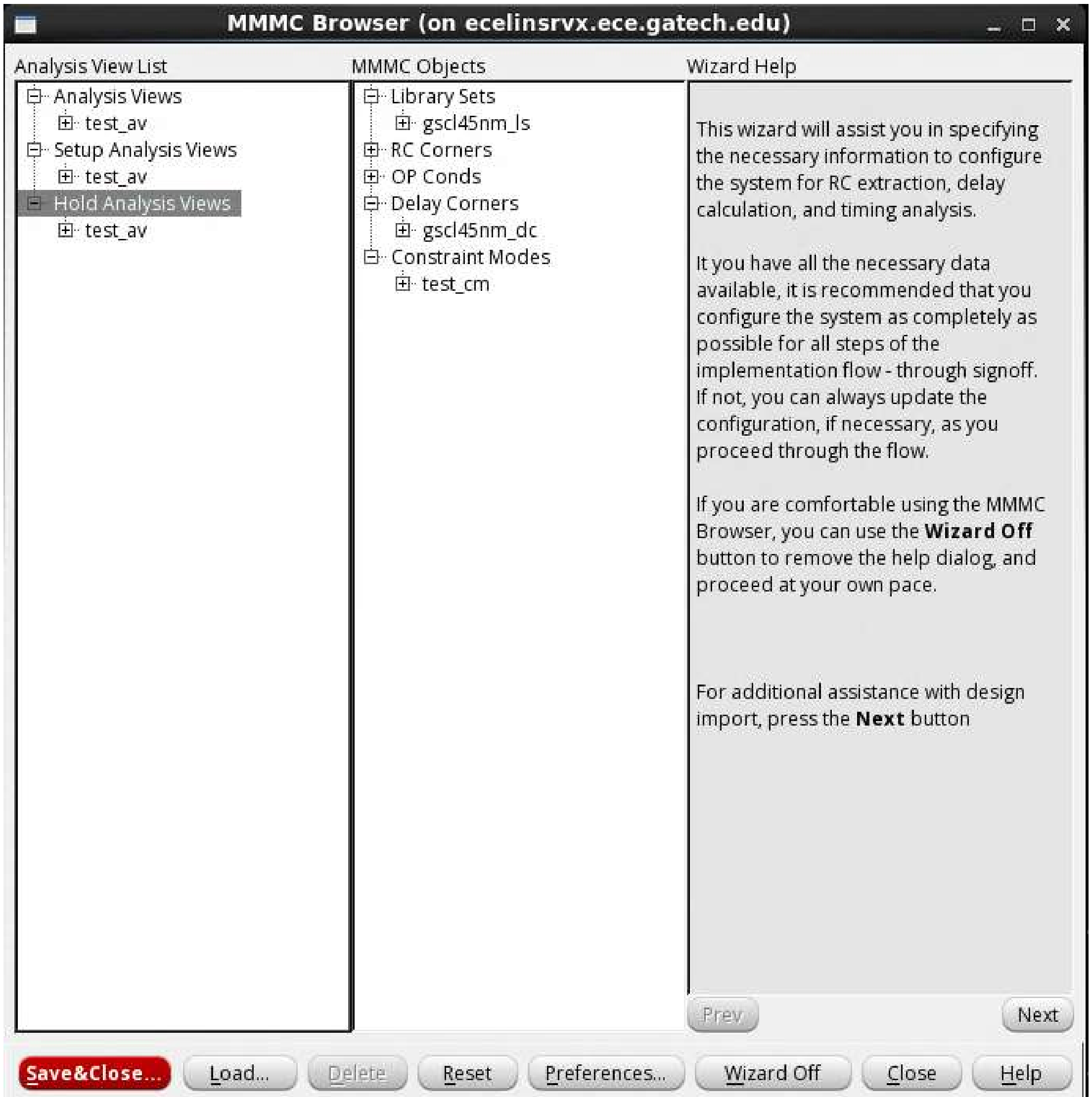


h) In MMMC Browser, double-click (e) “Setup Analysis Views” which opens “Add Setup Analysis View” window. Select (or confirm) “test_av” in Analysis View field. Click ‘OK’ to close the window.

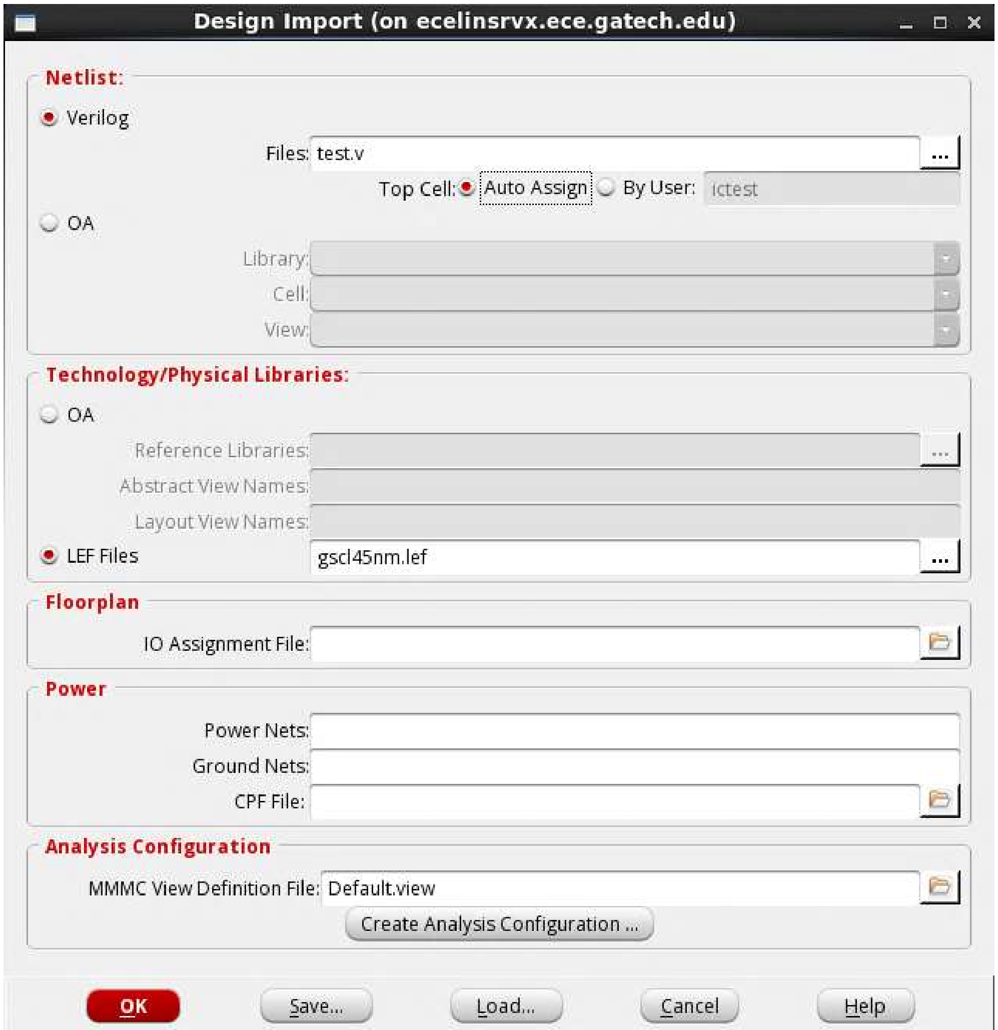
Do the same for (f) “Hold Analysis Views”.



i) The resulting MMMC Browser should look like the figure below. Click save & Close and save it as “Default.view”.



j) Your 'Design Import' window should look like the following.



k) Click 'OK' to import your design. Look at your command shell window. Innovus shows various information while it imports the design. The main window of Innovus will show you rows, where standard cells will be placed during placement.

2. Setting Up Layout Area

In this step, we will set up layout area. We will not do floorplanning.

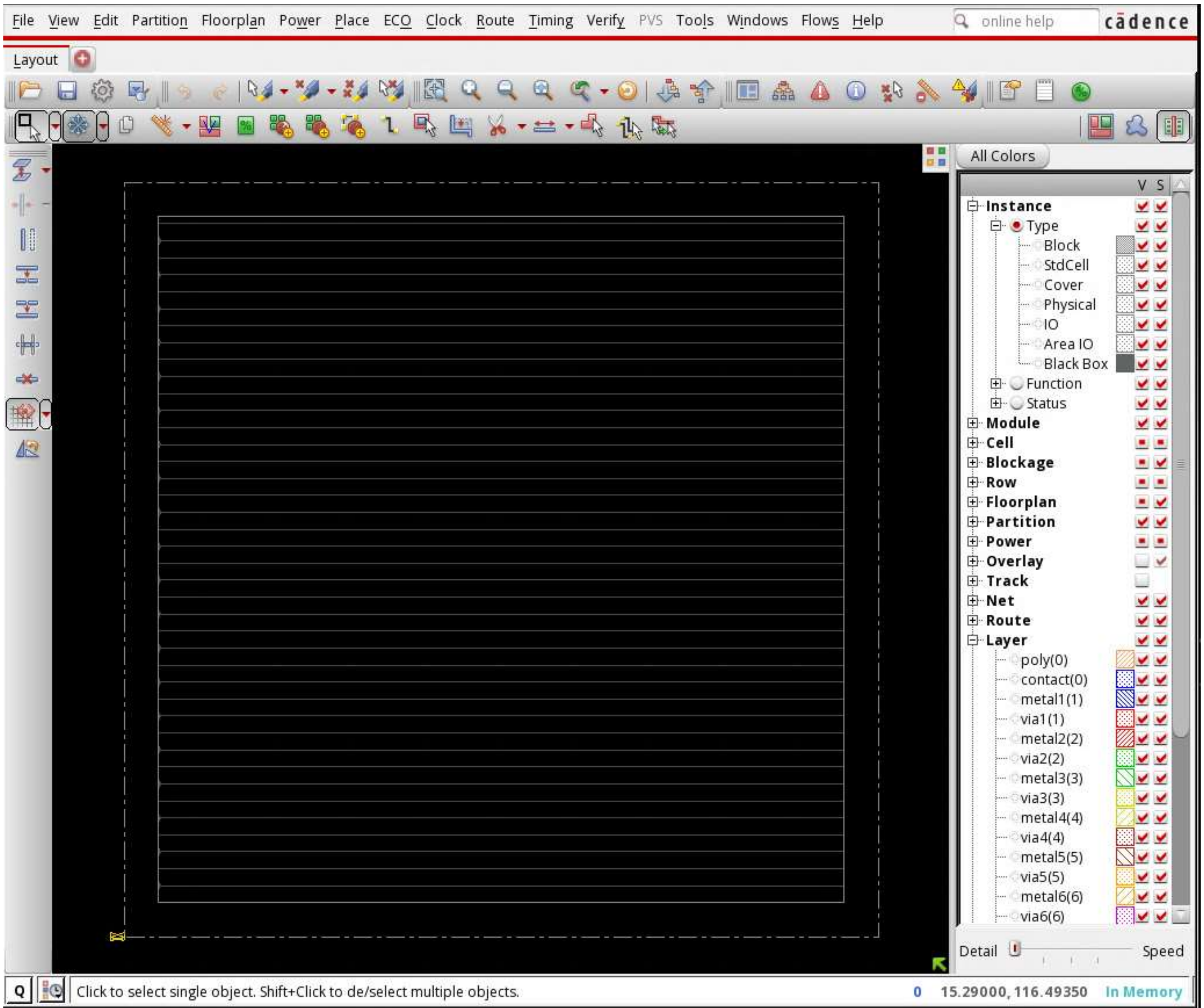
A. Choose 'Floorplan' and then 'Specify Floorplan ...' in the menu bar

B. In 'Basic' tab, you can specify core size by (1) AR (Aspect Ratio) or (2) Dimension. 'Core' is the region that cells are placed.

C. Choose 'Dimension' under 'Core Size by’ and set width and height to be 100. (100 by 100 is actually too large for this design. You will be asked to change the width and height later.)

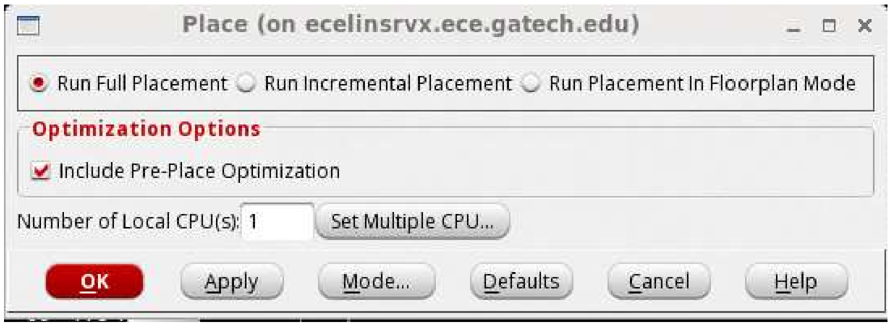
D. Choose 'Core to IO Boundary' and set 'Core to Left', 'Core to Top', 'Core to Right' and 'Core to Bottom' to 5

E. Click 'OK' to finish and see the modified floorplan outline in the main window. It should look like the following.



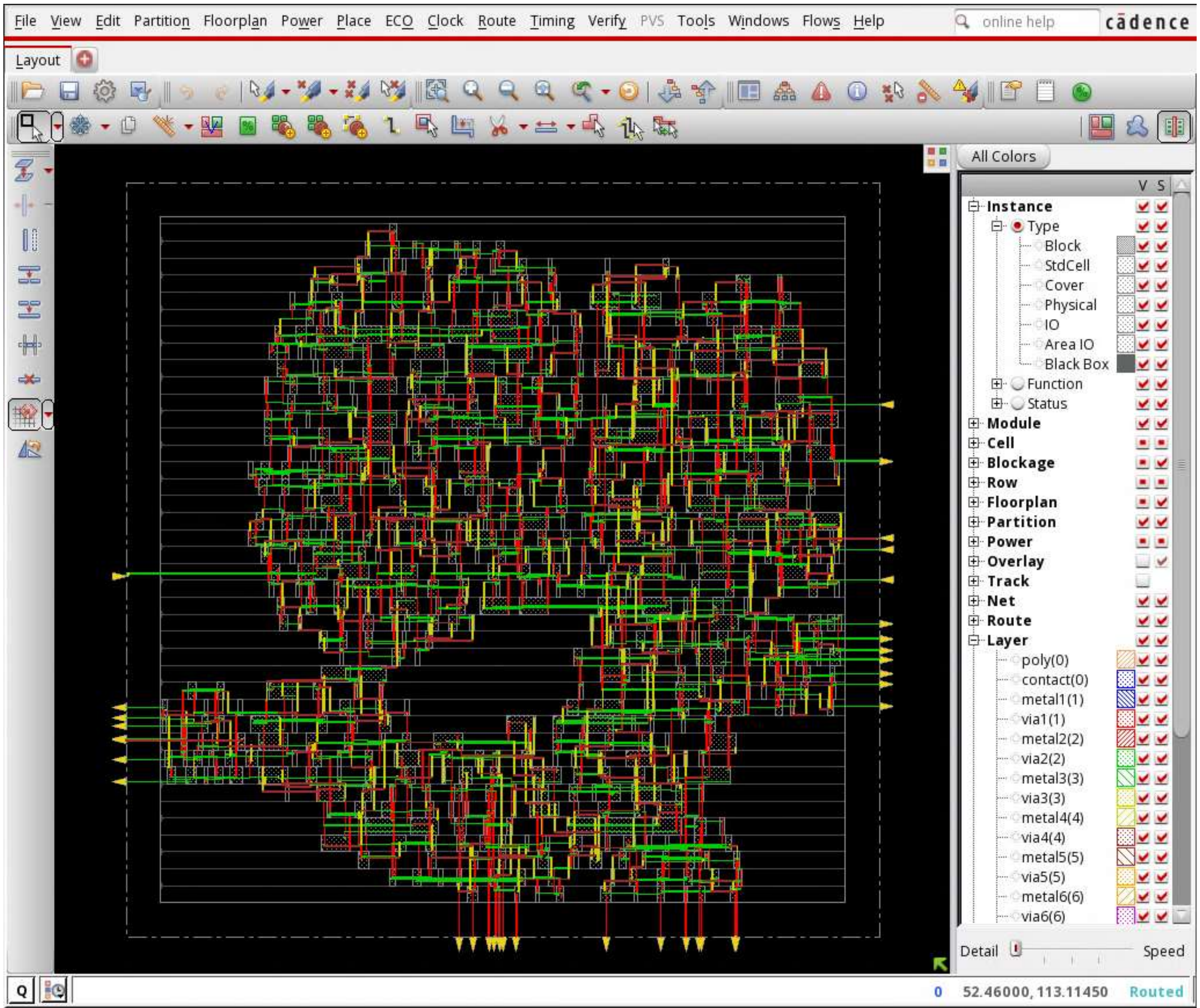
3. Performing Placement

A. Choose 'Place' -> 'Place Standard Cell…' then you will see the following window.



B. Click 'Mode…', click "Set Defaults", and click "OK".

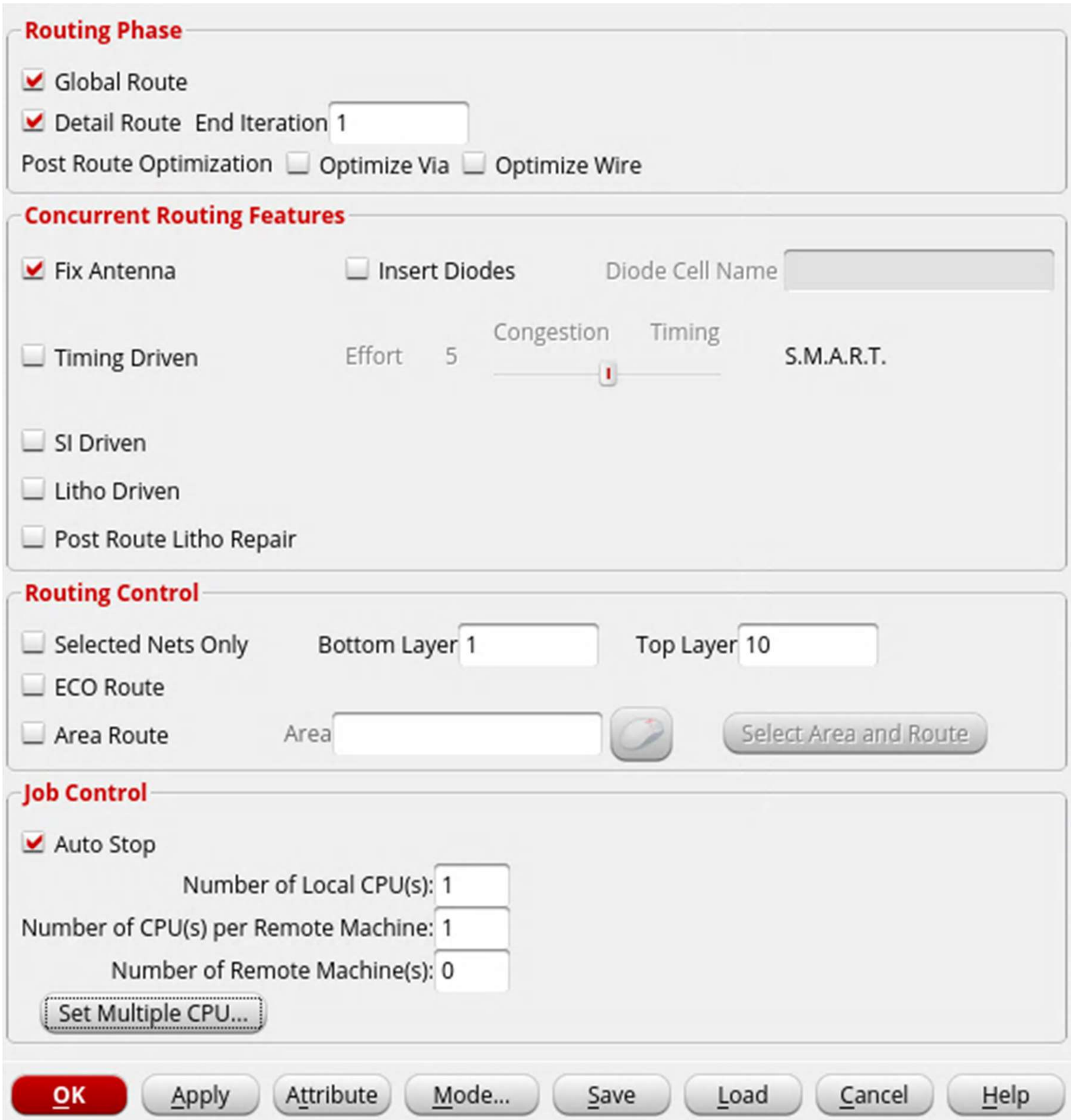
C. In Place Window, click 'OK" to perform placement. Innovus will do placement as well as trial-routing (It is not actual routing)



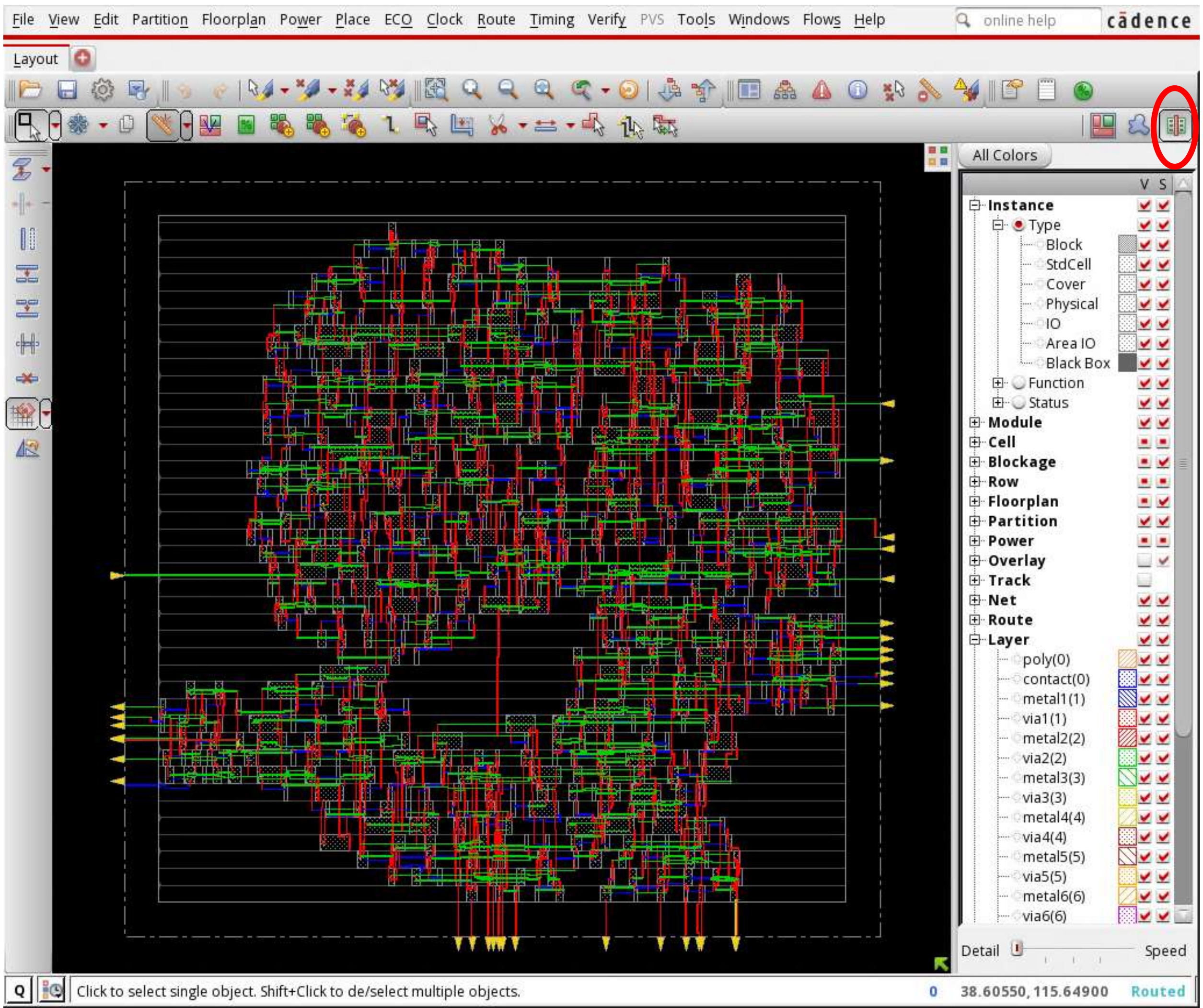
D. To see the core utilization, click '%' button in the toolbar and drag and make a rectangle containing the core region. The utilization will be shown in your command shell window. It will be about 22.1% in this example.

4. Performing Routing

A. Choose 'Route' -> 'Nanoroute' -> 'Route...' then you will see the following window.



B. Click 'OK' to do routing with default settings. Click 'Physical view' button (highlighted with red circle in the following window) and see the routing result. It should look like the following.

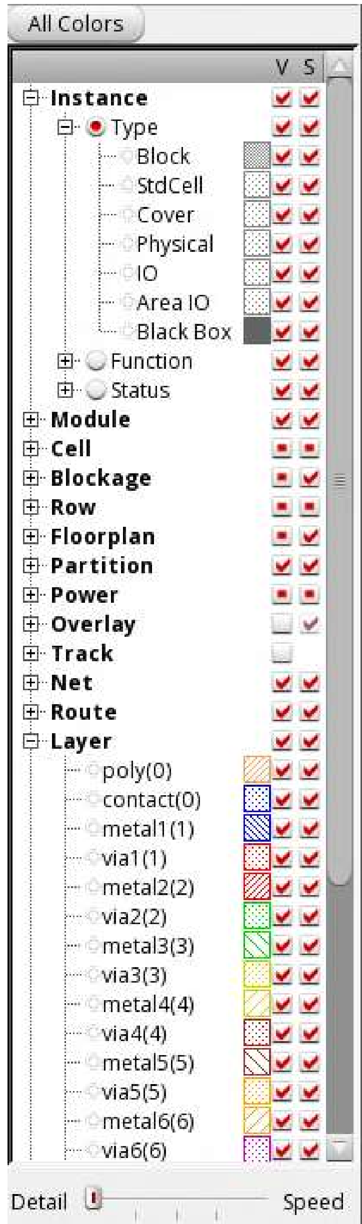


C. See your command shell window. It shows the routing information such as total wirelength, total wirelength in each metal layer, the number of vias, the number of DRC violations, and so on.

D. How to capture screenshots: Choose 'Tools' -> 'Screen Capture' -> “Write To GIF File…”

5. How to View Specific Metal Layers and Vias

On the right side of the screen, scroll down and see the following items.



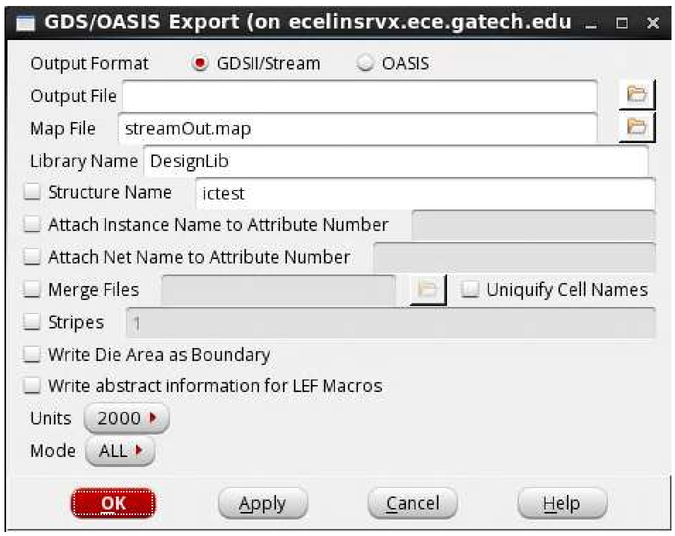
You can turn on and off the visibilities of metal layers and vias. Turn on and off visibilities and see if it works well. You will need this to capture specific metal layers later.

III. GDSII File Generation

After finishing up to routing step, you have to save your design to make a final layout which includes layouts of standard cells. This step is done by Cadence Virtuoso, thus you have to save your design and load it in Virtuoso. We will use gdsii format for this.

1. GDS Export

Choose 'File' -> 'Save' -> 'GDS/OASIS…' then you will see the following window.

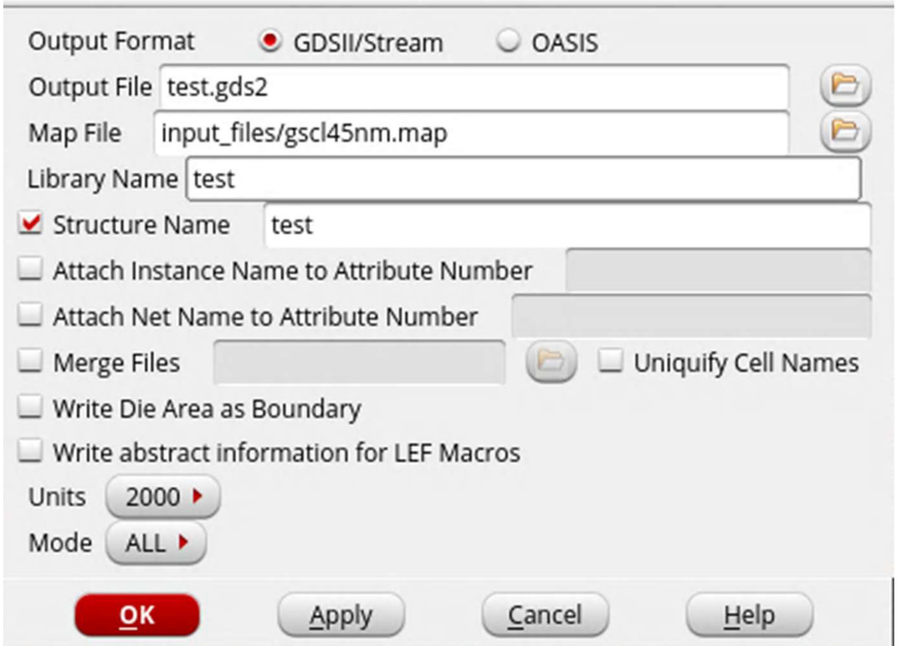


2. Setting

Use the following setting:

- Output Format : GDSII/Stream
- Output File : type a file name for gdsii output file.
- Map File : choose 'gscl45nm.map'
- Library Name : test (for test.v), IC1 (for IC1.v), IC2 (for IC2.v), IC3 (for IC3.v)
- GDS Structure Name : same as Library Name

The GDS Export window should look like the following.

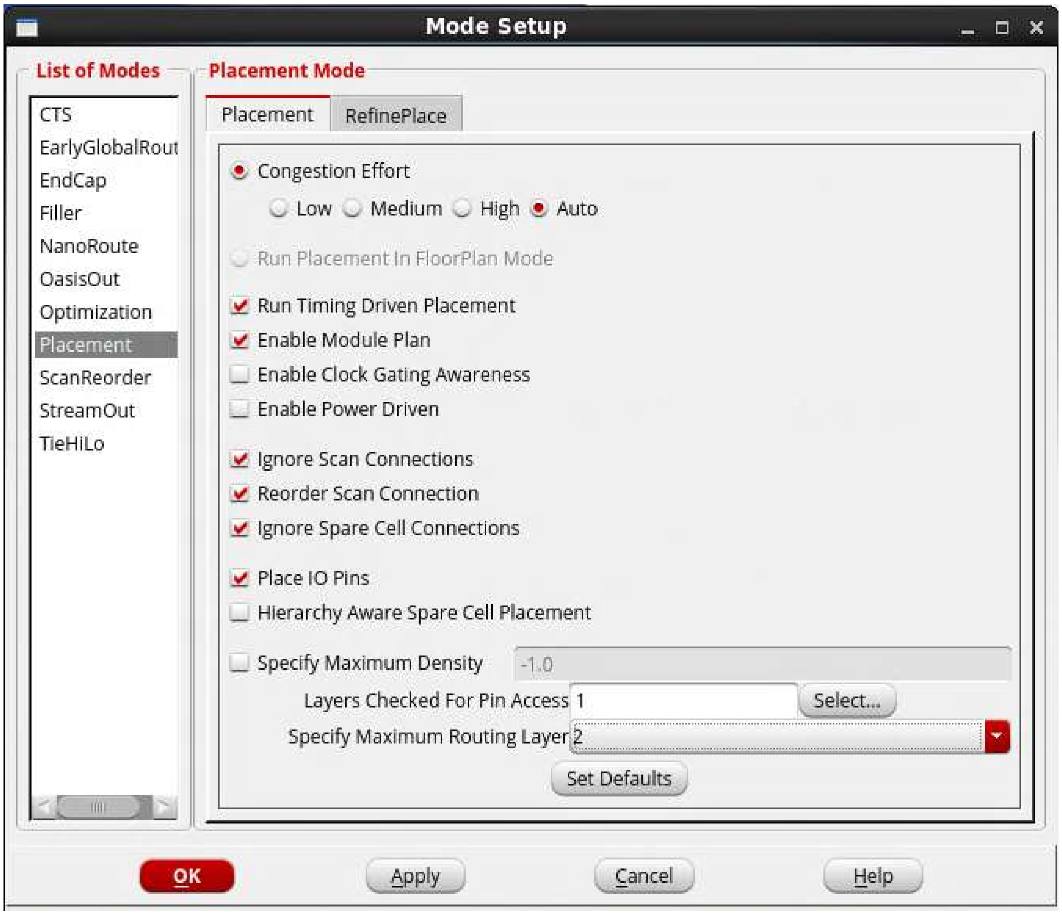


Click 'OK' to save your design.

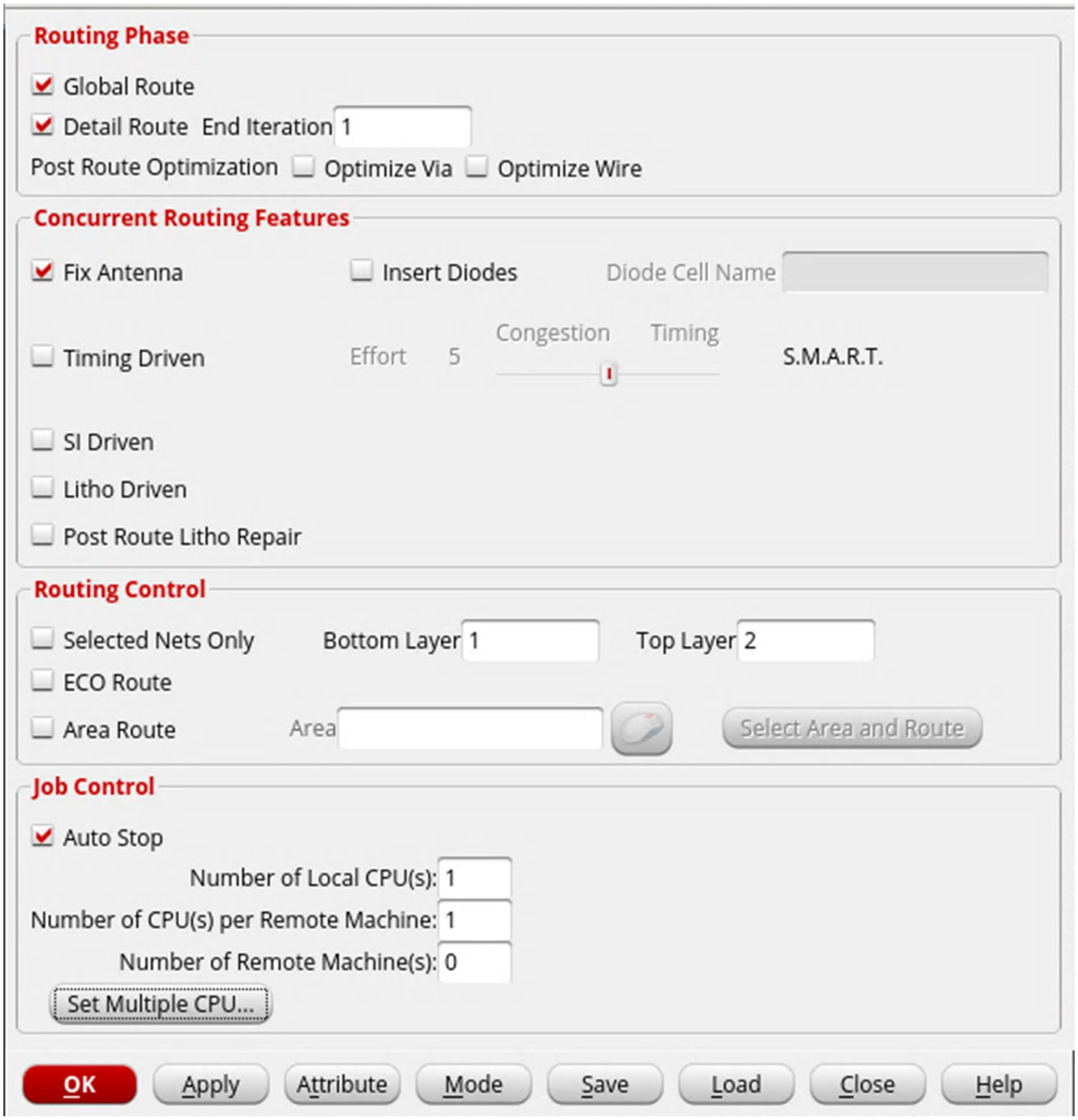
IV. Exercise

Try these to enhance your understanding of Cadence Innovus. You don't need to submit the answers to these items.

1. Try the whole step with the same netlist file (test.v) and the modified core area (30x30). You don't need to turn off and on Innovus. Just start from '2.2 setting-up of layout area' step. After placement is done, check out your command shell window. You will see error messages because core area is too small.
2. Try the whole step with the same netlist file with the modified core area (N by N). At this time, try with various N values and find the minimum N which passes placement and routing without any error.
3. “Specify Maximum Routing Layer” in placement step.
   In “Mode Setup” window (2.3.b in placement step), Set “Specify Maximum Routing Layer” as 2.



After placement is done, open NanoRoute window and set 'Top Layer' in 'Routing Control' box. The value in 'Top Layer' box should be 2 which you specified during placement.



Run nanoroute and see the number of metal layers used in routing in your command shell window.