Curriculum Vitae

Dr. Sung Kyu Lim
Motorola Solutions Foundation Professor
School of Electrical and Computer Engineering
Georgia Institute of Technology
IEEE Fellow

1 Career Highlights

1.1 Research

1. Donald O. Pederson Best Paper Award, IEEE Transactions on Computer-Aided Design (2022). The flagship journal in Electronic Design Automation (EDA).

2. Best Paper Award, ACM Design Automation Conference (2023). Out of 1,157 submissions. The flagship conference in Electronic Design Automation (EDA).

1.2 Teaching

1. Undergrad teaching: "ECE2020: Introduction to Computer Engineering" at Georgia Tech

    - Required class for freshmen at the School of Electrical and Computer Engineering
    - I received the Class of 1940 Course Survey Teaching Effectiveness Award five times (2016, 2018, 2019, 2020, 2022), the institute-level annual teaching award based on student course survey.
    - Average teaching rate over 46 offerings: 4.76 out of 5.0.

2. Graduate teaching: "ECE6133: Physical Design Automation of VLSI Systems" at Georgia Tech

    - Developed in 2001 and taught annually at Georgia Tech. The course has not been offered since Fall 2022 due to my appointment at DARPA.
    - World's largest graduate-level course solely devoted to Physical Design Automation.
    - Registered students total during the last 3 offerings: Spring 2019 (76), Spring 2021 (60 during COVID), Spring 2022 (84). Photos available at the course website: https://limsk.ece.gatech.edu/course/ece6133
    - Average teaching rate over 19 offerings: 4.8 out of 5.0.

1.3 Positions and Recognition

1. Dan Fielder Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology (2014 – 2019)

2. Motorola Solutions Foundation Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology (2022 – 2027)

3. IEEE Fellow for "contributions to electronic design automation and tradeoff for 3-dimensional integrated circuits," (2023 – present)

4. Program Manager, Microsystems Technology Office (MTO), Defense Advanced Research Projects Agency (DARPA) (2022 – 2024). Recruited to build and manage Electronic Design Automation (EDA) programs.

2 Earned Degrees

1. BS: University of California at Los Angeles, Computer Science Department (1994)
2. MS: University of California at Los Angeles, Computer Science Department (1997)
3. PhD: University of California at Los Angeles, Computer Science Department (2000)

3 Employment

1. Graduate Research Assistant, UCLA VLSI CAD Lab (September 1995 – June 2000)
2. Post Doctoral Scholar, UCLA VLSI CAD Lab (September 2000 – June 2001)
3. Assistant Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology (August 2001 – July 2007)
4. Associate Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology (August 2007 – July 2013)
5. Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology (August 2013 – current)
6. Dan Fielder Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology (July 2014 – June 2019)
7. Motorola Solutions Foundation Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology (April 2022 – March 2027)
8. Program Manager, Microsystems Technology Office (MTO), Defense Advanced Research Projects Agency (DARPA) (August 2022 – July 2024)

Other Appointments

1. Senior Engineer, Aplus Design Technologies, Inc. (June 2000 – June 2001)
2. Visiting Scholar, School of Electrical Engineering and Computer Science, Seoul National University (Summer 2001)
3. Instructor, Department of Electrical Engineering, Korean Advanced Institute of Science and Technology (KAIST), (Summer 2007)
4. Instructor, Department of Computer Science, Korea University (Summer 2007, Summer 2008, Summer 2009, Summer 2010)
5. Visiting Professor, Corporate Research and Development, Qualcomm Inc, San Diego (Summer 2014)
6. Visiting Professor, System LSI, Samsung Electronics, Hwasung, South Korea (Summer 2021)

4 Teaching

4.1 Individual Student Guidance

4.1.1 Graduated PhD Students

1. Mongkol Ekpanyapong, "Microarchitecture-Aware Physical Planning for Deep Submicron Technology," 2005. Tenure-track faculty at the Asian Institute of Technology, Thailand.
2. Jacob Minz, "Physical Design Automation for System-on-Packages (SOP) and 3D-ICs," 2006. Synopsys.

3. Ismail Faik Baskaya, “Physical Synthesis for Field Programmable Analog Array,” 2009. Tenure-track faculty at Bogazici University, Turkey.
4. Michael Healy, “Physical Design For Performance and Thermal and Power-Supply Reliability in Modern 2D And 3D Microarchitectures,” 2010. IBM T. J. Watson Research Center.
5. Dae Hyun Kim, “TSV-aware System-level Prediction and Physical Design for Multi-granularity 3D ICs,” 2012. Tenure-track faculty at the Washington State University, USA.
6. Krit Athikulwongse, “Placement for Fast and Reliable Through-Silicon Via (TSV) Based 3D-IC Layouts,” 2012. The National Electronics and Computer Technology Center, Thailand.
7. Xin Zhao, “Reliable Clock and Power Delivery Network Design for 3D ICs,” 2012. IBM.
8. Young Joon Lee, “CAD Methodologies for Low Power and Reliable 3D ICs,” 2013. Google.
9. Moongon Jung, ”Low Power and Reliable Design Methodologies for 3D ICs,” 2014. Intel.
10. Shreepad Panth, “Physical Design Methodologies for Monolithic 3D ICs,” 2015. Intel.
11. Taigon Song, “Chip/Package Co-design Methodologies for Reliable 3D ICs,” 2015. Tenure-track faculty at Kyungbook National University.
12. Yarui Peng, “CAD Tools and Methodologies for Reliable 3D IC Design, Analysis, and Optimization,” 2016. Tenure-track faculty at the University of Arkansas, USA.
13. Sandeep Samal, “Design Challenges and CAD Solutions for Low Power and Reliable Monolithic 3D ICs,” 2017. Intel.
14. Kyungwook Chang, “Design and Tool Solutions for Energy-Efficient Reliable Monolithic 3D ICs,” 2019. Tenure-track faculty at Sungkyunkwan (SKK) University.
15. Bon Woong Ku, “Physical Design Solutions For 3D ICs and their Neuromorphic Applications,” 2019. Synopsys.
16. Anthony Agnesina, “Electronic Design Automation for High-Performance and Reliable 3D Memory Cubes and Processors,” 2022. NVIDIA.
17. Jinwoo Kim, “Electronic Design Automation Solutions and Design Tradeoffs for Emerging Heterogeneous 2.5D and 3D ICs,” 2022. Intel.
18. Sai Pentapati, “Electronic Design Automation Tools and Design Study for Heterogeneous Monolithic 3D Integrated Circuits,” 2022. Intel.
19. Yi-Chen Lu, ”Machine Learning in Physical Design for 2D and 3D Integrated Circuits,” 2023. Apple.
20. Da Eun Shim, “Exploration, Modeling and Optimization of Advanced Interconnects: Solutions to Node Scaling Challenges,” 2023. Intel. (co-advised with Prof. Azad Naeemi)
21. Lingjun Zhu, “Power Delivery and Thermal-Aware Electronic Design Automation Solutions for High-Performance 3D ICs,” 2023. Apple.
22. Gauthaman Murali, “Design Methodologies of 2.5D and 3D Near-memory and In-memory Compute ML Accelerators,” 2023. Intel.
23. Pruek Vanna-iampikul, “Design Algorithms and Methodologies for Heterogeneous 2.5D and 3D Integrated Circuits,” 2024. Burapha University, Thailand.

4.1.2 Current PhD Students

1. Hao-Hsiang Hsiao
2. Yen-Hsiang Huang
3. Hang Yang (co-advised with Prof. Callie Hao)
4. Amaan Rahman
5. Jiawei Hu
6. Junyoung Hwang
7. Min Gyu Park
8. Seungmin Woo
9. Sungwoo Jung
10. Zheng Yang
11. Jae Hyung Ju
12. Yuan-Hsiang Lu
13. Cheng-Yu Tsai
14. Juyeop Baek
15. Karthic Palaniappan

4.1.3 Graduated MS Students (Thesis Option)

1. Ramprasad Ravichandran, "Placement for Quantum Cell Automata-based Circuits," 2005.
2. Hemant Sane, "Power Supply Noise Analysis For 3D ICs Using Through-Silicon-Vias," 2010.
3. Neela Lohith, "Monolithic 3D Integration of Asynchronous Systems," 2014.
4. Mohit Pathak, "Performance and Reliability-aware Physical Design for 3D IC and Package," 2014.
5. Rakesh Perumal, "Power and Performance Optimization of Negative Capacitance Transistor Circuits," 2018.
6. Nesara Bethur, "A Methodology for Back-side Clock Delivery Network Design Compatible with Commercial EDA Flows," 2023.
7. Sandra Shaji, "3nm Nanosheet FET vs. FinFET Comparison and Optimization with device/circuit co-design framework," 2023.
8. Aditya Iyer, "A Physical Design Framework for Creating Fine-Grained Multi-Tier SRAM Arrays," 2024.

4.2 Other Teaching Activities

4.2.1 New Graduate Course Development

Physical Design Automation of VLSI Systems: This course was offered in Summer 2002, Fall 2003, and Spring 2005 as a special topics course and became a permanent graduate course (ECE6133) in the School of Electrical and Computer Engineering.

- Description: The objective of physical design automation is to transform a structural representation of a VLSI system into a layout representation so that the resulting layout satisfies topological, geometric, timing, and power-consumption constraints of the design. This course focuses on various design automation problems in the physical design process of VLSI circuits, including: logic partitioning, floorplanning, global routing, detailed routing, compaction, and performance-driven layout. In addition, the discussion of a number of important optimization techniques, such as network flow, Steiner tree, scheduling, simulated annealing, generic algorithm, and linear/convex programming are included.
- Motivation: A significant portion of today's VLSI chips is designed with automatic layout generation tools. This is the first course ever offered at the Georgia Institute of Technology that teaches VLSI layout automation.

5 Scholarly Accomplishments

5.1 Published Books

1. Sung Kyu Lim, "Practical Problems in VLSI Physical Design Automation," Springer, July 2008. (ISBN 978-1-4020-6626-9)
2. Sung Kyu Lim, "Design for High Performance, Low Power, and Reliable 3D Integrated Circuits," Springer, December 2012. (ISBN 978-1-4419-9541-4)

5.2 Book Chapters

1. Sung Kyu Lim and Mike Niemier, "Partitioning and Placement for Buildable QCA Circuits," in *Nano, Quantum and Molecular Computing: Implications to High Level Design and Validation*, edited by Sandeep Shukla and Iris Bahar, Springer, pp 295-316, June 2004. (ISBN 978-1-4020-8067-8)
2. Young-Joon Lee, Michael Healy, and Sung Kyu Lim, "Co-optimization of Power, Thermal, and Signal Interconnect for 3D ICs," in *Three Dimensional System Integration: IC Stacking Process and Design*, edited by Antonis Papanikolaou, Dimitrios Soudris and Riko Radojcic, Springer, 2010. (ISBN 978-1-4419-0961-9)
3. Dae Hyun Kim and Sung Kyu Limm, "Impact of TSV and Device Scaling on the Quality of 3D ICs," in *More than Moore Technologies for Next Generation Computer Design*, edited by Rasit Topaloglu, Springer, 2015 (ISBN 978-1-4939-2163-8).
4. Sandeep Samal and Sung Kyu Lim, "Ultra-low Power Processor Design with 3D IC Operating at Sub/Near-threshold Voltages," in *CISS: Nano Devices and Circuit Techniques for Low-Energy Applications and Energy Harvesting*, edited by Chong-Min Kyung, Springer, 2015 (ISBN 978-9-4017-9990-4)
5. Sung Kyu Lim, "3D Interconnect Extraction," in *Physical Design for 3D Integrated Circuits*, edited by Aida Todri-Sanial and Chuan Seng Tan, CRC Press, 2015. (ISBN 978-1-4987-1036-7)
6. Sung Kyu Lim and Yiyu Shi, "Design Challenges and Solutions for Monolithic 3D ICs," in *Physical Design for 3D Integrated Circuits*, edited by Aida Todri-Sanial and Chuan Seng Tan, CRC Press, 2015. (ISBN 978-1-4987-1036-7)
7. Sung Kyu Lim, "Physical Design for 3D ICs," in *Electronic Design Automation for Integrated Circuits Handbook*, edited by Luciano Lavagno, Grant Martin, and Igor Markov, CRC Press, 2016. (ISBN 978-1-4822-5460-0)
8. Sandeep Samal and Sung Kyu Lim, "Design and CAD Solutions for Cooling and Power Delivery for Monolithic 3D-ICs," in *Handbook of 3D Integration, Volume 4: Design, Test, and Thermal Management*, edited by Paul Franzon, et al, Wiley-VCH, 2019. (ISBN 978-3-5273-3855-9).
9. Anthony Agnesina, Yi-Chen Lu, and Sung Kyu Lim, "Circuit Optimization for 2D and 3D ICs with Machine Learning," in Machine Learning Applications in Electronic Design Automation, edited by Haoxing Ren and Jiang Hu, Springer, 2023. (ISBN 978-3-031-13073-1).

10. Kyungwook Chang and Sung Kyu Lim, "Design and Tool Solutions for Monolithic Three-Dimensional Integrated Circuits," in Handbook of Computer Architecture, Springer, 2024. (ISBN 978-981-15-6401-7).

5.3 Refereed Publications

5.3.1 Refereed Journal Publications

1. Jason Cong and Sung Kyu Lim, "Edge Separability based Circuit Clustering With Application to Multi-level Circuit Partitioning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 23, No. 3, pp. 346-357, 2004.

2. Jason Cong and Sung Kyu Lim, "Retiming-based Timing Analysis With An Application to Mincut-based Global Placement," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 23, No. 12, pp. 1684-1692, 2004.

3. Ramprasad Ravichandran, Sung Kyu Lim, and Michael Niemier, "Automatic Cell Placement for Quantum-dot Cellular Automata," *Integration, the VLSI Journal*, Vol. 38, No. 3, pp. 541-548, 2005.

4. Sung Kyu Lim, Ramprasad Ravichandran, and Mike Niemier, "Partitioning and Placement for Buildable QCA Circuits," *ACM Journal on Emerging Technologies in Computing Systems*, Vol. 1, No. 1, pp. 50-72, 2005.

5. Sung Kyu Lim, "Physical Design for 3D System-On-Package: Challenges and Opportunities," *IEEE Design & Test of Computers*, Vol. 22, No. 6, pp. 532-539, 2005.

6. Peter Sassone and Sung Kyu Lim, "Traffic: A Novel Geometric Algorithm For Fast Wire-Optimized Floorplanning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 6, pp. 1075-1086, 2006.

7. Mongkol Ekpanyapong, Jacob Minz, Thaisiri Watewai, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Profile-Guided Microarchitectural Floorplanning for Deep Submicron Processor Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 7, pp. 1289-1300, 2006.

8. Eric Wong, Jacob Minz, and Sung Kyu Lim, "Thermal and Power Integrity-aware Module Placement For 3D System-On-Package," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 14, No. 5, pp. 553-557, 2006.

9. Faik Baskaya, Sasank Reddy, Sung Kyu Lim, and David Anderson, "Placement for Large-Scale Floating Gate Field-Programable Analog Arrays," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 14, No. 8, pp. 906-910, 2006.

10. Jacob Minz, Eric Wong, Mohit Pathak, and Sung Kyu Lim, "Placement and Routing for 3D System-On-Package Designs," *IEEE Transactions on Components and Packaging Technologies*, Vol. 29, No. 3, pp. 644-657, 2006.

11. Jacob Minz and Sung Kyu Lim, "Block-level 3D Global Routing With an Application to 3D Packaging," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 10, pp. 2248-2257, 2006.

12. Wook-Jin Chung, Brian Smith, and Sung Kyu Lim, "Node Duplication and Routing Algorithms for Quantum-dot Cellular Automata Circuit," *IEE Proceedings on Circuits, Devices & Systems*, Vol. 153, No. 5, pp. 497-505, 2006.

13. Mongkol Ekpanyapong, Michael Healy, and Sung Kyu Lim, "Profile-Driven Instruction Mapping for Dataflow Architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 12, pp. 3017-3025, 2006.

14. Michael Healy, Mario Vittes, Mongkol Ekpanyapong, Sung Kyu Lim, Hsien-Hsin S. Lee, and Gabriel H. Loh, "Multi-Objective Microarchitectural Floorplanning For 2D And 3D Stacked ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 1, pp. 38-52, 2007.

15. Jacob Minz, Somaskanda Thyagaraja, and Sung Kyu Lim, "Optical Routing for 3D System-On-Package," *IEEE Transactions on Components and Packaging Technologies*, Vol. 30, No. 4, pp. 805-812, 2007.

16. Eric Wong, Jacob Minz, and Sung Kyu Lim, "Decoupling Capacitor Planning and Sizing for Noise and Leakage Reduction," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 11, pp. 2023-2034, 2007.

17. Faik Baskaya, David V. Anderson, and Sung Kyu Lim, "Net Sensitivity Based Optimization of Large-scale Field Programmable Analog Array (FPAA) Placement and Routing," *IEEE Transactions on Circuits and Systems II*, Vol. 56, No. 7, pp. 565-569, 2009.

18. Mohit Pathak and Sung Kyu Lim, "Performance and Thermal-aware Steiner Routing for 3D Stacked ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 28, No. 9, pp. 1373-1386, 2009.

19. Yoon Jo Kim, Yogendra K. Joshi, Andrei G. Fedorov, Young-Joon Lee, and Sung Kyu Lim, "Thermal Characterization of Interlayer Microfluidic Cooling of Three-Dimensional IC with Non-Uniform Heat Flux," *ASME Journal of Heat Transfer*, Vol. 132(4), pp. 1-9, 2010.

20. Muhammad Bashir, Linda Milor, Dae Hyun Kim, and Sung Kyu Lim, "Methodology to Determine the Impact of Linewidth Variation on Chip Scale Copper/Low-k Backend Dielectric Breakdown," *Elsevier Microelectronics Reliability*, Vol. 50, Issue 9-11, pp. 1341-1346, 2010.

21. Dae Hyun Kim, Saibal Mukhopadhyay, and Sung Kyu Lim, "Fast and Accurate Analytical Modeling of Through-Silicon-Via Capacitive Coupling," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 1, No. 2, pp. 168-180, 2011.

22. Xin Zhao, Jacob Minz, and Sung Kyu Lim, "Low-Power and Reliable Clock Network Design for Through Silicon Via based 3D ICs," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 1, No. 2, pp. 247-259, 2011.

23. Xin Zhao, Dean L. Lewis, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Low-Power Clock Tree Design for Pre-Bond Testing of 3D Stacked ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 30, No. 5, pp. 732-745, 2011.

24. Jeremy Tolbert, Xin Zhao, Sung Kyu Lim, and Saibal Mukhopadhyay, "Analysis and Design of Energy and Slew Aware Subthreshold Clock Systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 30, No. 9, pp. 1349-1358, 2011.

25. Muhammad Bashir, Linda Milor, Dae Hyun Kim, and Sung Kyu Lim, "Impact of Irregular Geometries on Low-k Dielectric Breakdown," *Microelectronics Reliability*, Vol. 51, No. 9-11, pp. 1582-1586, 2011.

26. Michael Healy, Fayez Mohamood, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Integrated Microarchitectural Floorplanning and Runtime Controller for Inductive Noise Mitigation," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 14, No. 4, pp. 1-25, 2011.

27. Young-Joon Lee and Sung Kyu Lim, "Co-Optimization and Analysis of Signal, Power, and Thermal Interconnects in 3D ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 30, No. 11, pp. 1635-1648, 2011.

28. Minki Cho, Chang Liu, Dae Hyun Kim, Sung Kyu Lim, and Saibal Mukhopadhyay, "Pre-bond and Post-bond Test and Signal Recovery Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3D System," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 1, No. 11, pp. 1718-1727, 2011.

29. Mohit Pathak and Sung Kyu Lim, "Fast Layout Generation of RF Embedded Passive Circuits Using Mathematical Programming," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 2, No. 1, pp. 32-45, 2012.

30. Michael B. Healy and Sung Kyu Lim, "Distributed TSV Topology for 3D Power-Supply Networks," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 20, No. 11, pp. 2066-2079, 2012.

31. Moongon Jung, Joydeep Mitra, David Pan, and Sung Kyu Lim, "TSV Stress-aware Full-Chip Mechanical Reliability Analysis and Optimization for 3D IC," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 31, No. 8, pp. 1194-1207, 2012.

32. Xin Zhao, Jeremy Tolbert, Saibal Mukhopadhyay, and Sung Kyu Lim, "Variation-aware Clock Network Design Methodology for Ultra-Low Voltage (ULV) Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 31, No. 8, pp. 1222-1234, 2012.

33. Dae Hyun Kim and Sung Kyu Lim, "Design Quality Trade-off Studies for 3D ICs Built with Sub-micron TSVs and Future Devices," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 2, No. 2, pp. 240-248, 2012.

34. Chang-Chih Chen, Fahad Ahmed, Dae Hyun Kim, Sung Kyu Lim, and Linda Milor, "Backend Dielectric Reliability Simulator For Microprocessor System," *Microelectronics Reliability*, Vol. 52, Issue 9-10, pp. 1953-1959, 2012.

35. Dae Hyun Kim, Krit Athikulwongse, and Sung Kyu Lim, "A Study of Through-Silicon-Via Impact on the 3D Stacked IC Layout," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 21, No. 5, pp. 862-874, 2013.

36. Junghee Lee, Chryostomos Nicopoulos, Hyung Gyu Lee, Shreepad Panth, Sung Kyu Lim, and Jongman Kim, "IsoNet: Hardware-based Job Queue Management for Manycore Architectures," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 21, No. 6, pp. 1080-1093, 2013.

37. Krit Athikulwongse, Jae-Seok Yang, David Z. Pan, and Sung Kyu Lim, "Impact of Mechanical Stress on the Full Chip Timing for TSV-based 3D ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 32, No. 6, pp. 905-917, 2013.

38. Kwanyeob Chae, Xin Zhao, Sung Kyu Lim, and Saibal Mukhopadhyay, "Tier-Adaptive-Body-Biasing: A Post-Silicon Tuning Method to Minimize Clock Skew Variations in 3D ICs," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 3, No. 10, pp. 1720-1730, 2013.

39. Moongon Jung, David Z. Pan, and Sung Kyu Lim, "Chip/Package Mechanical Stress Impact on 3D IC Reliability and Mobility Variations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 32, No. 11, pp. 1694-1707, 2013.

40. Sai Manoj, Hao Yu, Yang Shang, Chuan Seng Tan, and Sung Kyu Lim, "Reliable 3D Clock-tree Synthesis Considering Nonlinear Capacitive TSV Model with Electrical-thermal-mechanical Coupling," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 32, No. 11, pp. 1734-1747, 2013.

41. Young-Joon Lee and Sung Kyu Lim, "Ultra High Density Logic Designs using Monolithic 3D Integration," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.*, Vol. 32, No. 12, pp. 1892-1905, 2013.

42. Moongon Jung, Joydeep Mitra, David Z. Pan, and Sung Kyu Lim, "Full-Chip Mechanical Reliability Analysis and Optimization for 3D ICs," *Communications of the ACM*, Vol. 57, No. 1, pp. 107-115, 2014. **RESEARCH HIGHLIGHT.**

43. Xin Zhao, Michael Scheuermann, and Sung Kyu Lim, "Analysis and Modeling of DC Current Crowding for TSV-Based 3-D Connections and Power Integrity," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 4, No. 1, pp. 123-133, 2014.

44. Muhammad Bashir, Chang-Chih Chen, Linda Milor, Dae Hyun Kim, and Sung Kyu Lim, "Backend Dielectric Reliability Full Chip Simulator," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 22, No. 8, pp. 1750-1762, 2014.

45. Krit Athikulwongse, Mongkol Ekpanyapong, and Sung Kyu Lim, "Exploiting Die-to-Die Thermal Coupling in 3D IC Placement," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 22, No. 10, pp. 2145-2155, 2014.

46. Sung Kyu Lim, "Research Needs for TSV-Based 3D IC Architectural Floorplanning," *Journal of Information and Communication Convergence Engineering*, Vol. 12, No. 1, pp. 46-52, 2014.

47. Dae Hyun Kim, Saibal Mukhopadhyay, and Sung Kyu Lim, "TSV-Aware Interconnect Distribution Models for Prediction of Delay and Power Consumption of 3D Stacked ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 33, No. 9, pp. 1384-1395, 2014.

48. Shreepad Panth, Sandeep Samal, Yun Seop Yu, and Sung Kyu Lim, "Design Challenges and Solutions for Ultra-High-Density Monolithic 3D ICs," *Journal of Information and Communication Convergence Engineering*, Vol. 12, No. 3, pp. 186-192, 2014.

49. Yarui Peng, Taigon Song, Dusan Petranovic, and Sung Kyu Lim, "Silicon Effect-aware Full-chip Extraction and Mitigation of TSV-to-TSV Coupling," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 33, No. 12, pp. 1900-1913, 2014.

50. Jiwoo Pak, Sung Kyu Lim, and David Z. Pan, "Electromigration Study for Multi-scale Power/Ground Vias in TSV-based 3D ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 33, No. 12, pp. 46-52, 2014.

51. Brandon Noia, Shreepad Panth, Krishnendu Chakrabarty, and Sung Kyu Lim, "Scan Test of Die Logic in 3D ICs Using TSV Probing," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 23, No. 2, pp. 317-330, 2015.

52. Dae Hyun Kim, Krit Athikulwongse, Michael B. Healy, Mohammad M. Hossain, Moongon Jung, Ilya Khorosh, Gokul Kumar, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Shreepad Panth, Mohit Pathak, Minzhen Ren, Guanhao Shen, Taigon Song, Dong Hyuk Woo, Xin Zhao, Joungho Kim, Ho Choi, Gabriel H. Loh, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Design and Analysis of 3D-MAPS (3D Massively Parallel Processor with Stacked Memory)," *IEEE Transactions on Computers*, Vol. 64, No. 1, pp. 112-125, 2015.

53. Shreepad Panth, Kambiz Samadi, Yang Du, and Sung Kyu Lim, "Placement-Driven Partitioning for Congestion Mitigation in Monolithic 3D IC Designs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 34, No. 4, pp. 540-553, 2015.

54. Ahmet Ceyhan, Moongon Jung, Shreepad Panth, Sung Kyu Lim, and Azad Naeemi, "Evaluating Chip-Level Impact of Cu/low-k Performance Degradation on Circuit Performance at Future Technology Nodes," *IEEE Transactions on Electron Devices*, Vol. 62, No. 3, pp. 940-946, 2015.

55. Sandeep Samal, Yarui Peng, Mohit Pathak, and Sung Kyu Lim, "Ultra-Low Power Circuit Design with Sub/Near-Threshold 3D IC Technologies," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 5, No. 7, pp. 980 - 990, 2015.

56. Dae Hyun Kim and Sung Kyu Lim, "Design and CAD Tools for 3-D Integrated Circuits: Challenges and Opportunities," *IEEE Design and Test*, Vol. 32, No. 4, pp. 8-22, 2015.

57. Yarui Peng, Dusan Petranovik, and Sung Kyu Lim, "Multi-TSV and E-Field Sharing Aware Full-chip Extraction and Mitigation of TSV-to-wire Coupling," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 34, No. 12, pp. 1964-1976, 2015.

58. Moongon Jung, Taigon Song, Yarui Peng, and Sung Kyu Lim, "Fine-Grained 3D IC Partitioning Study with A Multi-core Processor," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 5, No. 10, pp. 1393-1491, 2015.

59. Taigon Song and Sung Kyu Lim, "Full-Chip Power/Performance Benefits of Carbon Nanotube-Based Circuits," *Journal of Information and Communication Convergence Engineering*, Vol. 13, No. 3, pp. 180-188, 2015.

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247. Anthony Agnesina, Moritz Brunion, Jinwoo Kim, Alberto Garcia-Ortiz, Dragomir Milojevic, Francky Catthoor, Manu Perumkunnil and Sung Kyu Lim, "Power, Performance, Area and Cost Analysis of Memory-on-Logic Face-to-Face Bonded 3D Processor Designs," *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2021. **NOMINATED FOR BEST PAPER AWARD.**

248. Lingjun Zhu, Saurabh Sinha, Tuan Ta, Rossana Liu, Rahul Mathur, Xiaoqing Xu, Shidhartha Das, Ankit Kaul, Alejandro Rico, Doug Joseph, Brian Cline and Sung Kyu Lim, "Power Delivery and Thermal-Aware Arm-Based Multi-Tier 3D Architecture," *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2021.

249. Sanmitra Banerjee, Arjun Chaudhuri, Jinwoo Kim, Gauthaman Murali, Marc Nelson, Sung Kyu Lim, and Krishnendu Chakrabarty, "ParaMitE: Mitigating parasitic CNFETs in the presence of unetched CNTs," *IEEE International Conference on Computer-Aided Design*, 2021.

250. Yi-Chen Lu, Siddhartha Nath, Vishal Khandelwal, and Sung Kyu Lim, "Doomed Run Prediction in Physical Design by Exploiting Sequential Flow and Graph Learning," *IEEE International Conference on Computer-Aided Design*, 2021.

251. Johann Knechtel, Jayanth Gopinath, Jitendra Bhandari, Mohammed Ashraf, Hussam Amrouch, Shekhar Borkar, Sung Kyu Lim, Ozgur Sinanoglu, and Ramesh Karri, "Security Closure of Physical Layouts," *IEEE International Conference on Computer-Aided Design*, 2021.

252. Yandong Luo, Sourav Dutta, Ankit Kaul, Sung Kyu Lim, Muhannad Bakir, Suman Datta, and Shimeng Yu, "Monolithic 3D Compute-in-Memory Accelerator with BEOL Transistor based Reconfigurable Interconnect," *IEEE International Electron Devices Meeting*, 2021. **INVITED PAPER.**

253. Matheus Cavalcante, Anthony Agnesina, Samuel Riedel, Moritz Brunion, Alberto Garcia-Ortiz, Dragomir Milojevic, Francky Catthoor, Sung Kyu Lim, and Luca Benini, "MemPool-3D: Boosting Performance and Efficiency of Shared-L1 Memory Many-Core Clusters with 3D Integration," *Design, Automation and Test in Europe*, 2022.

254. Gauthaman Murali, Sandra Maria Shaji, Anthony Agnesina, Guojie Luo, and Sung Kyu Lim, "ART-3D: Analytical 3D Placement with Reinforced Parameter Tuning for Monolithic 3D ICs," *ACM International Symposium on Physical Design*, 2022.

255. Sai Pentapati and Sung Kyu Lim, "Routing Layer Sharing: A New Opportunity for Routing Optimization in Monolithic 3D ICs," *ACM International Symposium on Physical Design*, 2022.

256. Anthony Agnesina, Moritz Brunion, Alberto Garcia-Ortiz, Francky Catthoor, Dragomir Milojevic, Manu Komalan, Matheus Cavalcante, Samuel Riedel, Luca Benini, and Sung Kyu Lim, "Hier-3D: A Hierarchical Physical Design Methodology for Face-to-Face Bonded 3D ICs," *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2022. **BEST PAPER AWARD.**

257. Lingjun Zhu, Nesara Bethur, Yi-Chen Lu, Youngsang Cho, Yunhyeok Im, and Sung Kyu Lim, "3D IC Tier Partitioning of Memory Macros: PPA vs. Thermal Tradeoffs," *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2022.

258. Yi-Chen Lu and Sung Kyu Lim, "On Advancing Physical Design using Graph Neural Networks," *IEEE International Conference on Computer-Aided Design*, 2022.

259. Yi-Chen Lu, Wei-Ting Chan, Vishal Khandelwal, and Sung Kyu Lim, "Driving Early Physical Synthesis Exploration through End-of-Flow Total Power Prediction," *ACM/IEEE Workshop on Machine Learning for CAD*, 2022

260. Yi-Chen Lu, Tian Yang, Sung Kyu Lim, and Haoxing Ren, "Placement Optimization via PPA-Directed Graph Clustering," *ACM/IEEE Workshop on Machine Learning for CAD*, 2022. **BEST STUDENT PAPER AWARD.**

261. Tathagata Srimani, Robert Radway, Jinwoo Kim, Kartik Prabhu, Dennis Rich, Carlo Gilardi, Priyanka Raina, Max Shulaker, Sung Kyu Lim, and Subhasish Mitra, "Ultra-Dense 3D Physical Design Unlocks New Architectural Design Points with Large Benefits," *Design, Automation and Test in Europe*, 2023.

262. Jonti Talukdar, Arjun Chaudhuri, Jinwoo Kim, Sung Kyu Lim, and Krishnendu Chakrabarty, "Securing Heterogeneous 2.5D ICs Against IP Theft through Dynamic Interposer Obfuscation," *Design, Automation and Test in Europe*, 2023.

263. Yi-Chen Lu, Haoxing Ren, Hao-Hsiang Hsiao, and Sung Kyu Lim, "DREAM-GAN: Advancing DREAMPlace towards Commercial-Quality using Generative Adversarial Learning," *ACM International Symposium on Physical Design*, 2023

264. Sai Pentapati, Yen-Hsiang Huang, and Sung Kyu Lim, "On Legalization of Die Bonding Bumps and Pads for 3D ICs," *ACM International Symposium on Physical Design*, 2023.

265. Narasinga Rao Miniskar, Pruek Vanna-iampikul, Aaron Young, Sung Kyu Lim, Frank Liu, Jieun Yoo, Corrinne Mills, Nhan Tran, Farah Fahim, and Jeffrey S. Vetter, "A 3D Implementation of Convolutional Neural Network for Fast Inference," *IEEE International Symposium on Circuits & Systems*, 2023.

266. Pruek Vanna-iampikul, Lingjun Zhu, Serhat Erdogan, Mohanalingam Kathaperumal, Ravi Agarwal, Ram Gupta, Kevin Rinebold, and Sung Kyu Lim, "Glass Interposer Integration of Logic and Memory Chiplets: PPA and Signal/Power Integrity Benefits," *ACM Design Automation Conference*, 2023.

267. Yi-Chen Lu, Wei-Ting Chan, Deyuan Guo, Sudipto Kundu, Vishal Khandelwal, and Sung Kyu Lim, "RL-CCD: Concurrent Clock and Data Optimization using Attention-Based Self-Supervised Reinforcement Learning," *ACM Design Automation Conference*, 2023. **BEST PAPER AWARD.**

268. Lingjun Zhu and Sung Kyu Lim, "Design Automation Needs for Monolithic 3D ICs: Accomplishments and Gaps," *ACM Design Automation Conference*, 2023. **INVITED PAPER.**

269. Sandra Shaji, Lingjun Zhu, Junsik Yoon, and Sung Kyu Lim, "A Comparative Study on Front-Side, Buried and Back-Side Power Rail topologies in 3nm Technology Node," *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2023.

270. Gauthaman Murali, Aditya Iyer, Navneeth Ravichandran and Sung Kyu Lim, "3DNN-Xplorer: A Machine Learning Framework for Design Space Exploration of Heterogeneous 3D DNN Accelerators," *IEEE/ACM International Conference On Computer-Aided Design*, 2023.

271. Hao-Hsiang Hsiao, Yi-Chen Lu, Pruek Vanna-Iampikul, and Sung Kyu Lim, "FastTuner: Transferable Physical Design Parameter Optimization using Fast Reinforcement Learning," *ACM International Symposium on Physical Design*, 2024.

272. Pruek Vanna-iampikul, Hang Yang, Jungyoun Kwak, Joyce X Hu, Amaan Rahman, Nesara Eranna Bethur, Cong Hao, Shimeng Yu, and Sung Kyu Lim, "A Design Methodology for Back-side Power and Clock Routing Co-Optimization," *IEEE Symposium on VLSI Technology & Circuits*, 2024.

273. Hao-Hsiang Hsiao, Pruek Vanna-iampikul, Yi-Chen Lu, and Sung Kyu Lim, "ML-based Physical Design Parameter Optimization for 3D ICs: From Parameter Selection to Optimization," *ACM Design Automation Conference*, 2024.

274. Nesara Eranna Bethur, Pruek Vanna-iampikul, Odysseas Zografos, Lingjun Zhu, Giuliano Sisto, Dragomir Milojevic, Alberto Garcia-Ortiz, Geert Hellings, Julien Ryckaert, Francky Catthoor, and Sung Kyu Lim, "GNN-assisted Back-side Clock Routing Methodology for Advance Technologies," *ACM Design Automation Conference*, 2024.

275. Lingjun Zhu, Jiawei Hu, Gauthaman Murali, and Sung Kyu Lim, "Hetero-3D: PPA and Power Delivery Benefits of Heterogeneous 3D ICs with a Customized Physical Design Flow", *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2024.

276. Aditya Iyer, Daehyun Kim, Saibal Mukhopadhyay, and Sung Kyu Lim, "Multi-Tier 3D SRAM Module Design: Targeting Bit-Line and Word-Line Folding", *IEEE/ACM International Conference on Computer-Aided Design*, 2024.

277. Boxun Xu, Junyoung Hwang, Pruek Vanna-iampikul, Sung Kyu Lim, and Peng Li, "Spiking Transformer Hardware Accelerators in 3D Integration", *IEEE/ACM International Conference on Computer-Aided Design*, 2024.

278. Seungmin Woo, Pruek Vanna-iampikul, and Sung Kyu Lim, "AI-Driven Evaluation and Optimization of Bump Pitch Effects on Chiplet and Interposer Design Quality", *IEEE/ACM International Conference on Computer-Aided Design*, 2024.

279. Zheng Yang, Zhen Zhuang, Bei Yu, Tsung-Yi Ho, Martin D.F. Wong, and Sung Kyu Lim, "ML-Based Fine-Grained Modeling of DC Current Crowding in Power Delivery TSVs for Face-to-Face 3D ICs", *ACM International Symposium on Physical Design*, 2025.

280. Pruek Vanna-iampikul, Junsik Yoon, Chaeryung Park, Gary Yeap, and Sung Kyu Lim, "Placement-Aware 3D Net-to-Pad Assignment for Array-Style Hybrid Bonding 3D ICs", *ACM International Symposium on Physical Design*, 2025.

5.4 Patents

1. Sung Kyu Lim and Yang Du, "Clock Skew Compensation with Adaptive Body Biasing in Three-Dimensional Integrated Circuits," **US Patent 9,256,246.**

2. Sung Kyu Lim, Kambiz Samadi, and Yang Du, "Intellectual Property Block Design With Folded Blocks and Duplicated Pins For 3D Integrated Circuits," **US Patent 9,483,598.**

3. Sung Kyu Lim, Kambiz Samadi, Pratyush Kamal, and Yang Du, "Clock Tree Synthesis for Low Cost Pre-Bond Testing of 3D Integrated Circuits," **US Patent 9,508,615.**

4. Sung Kyu Lim, Karam Chatha, Kambiz Samadi, and Yang Du, "Memory Controller Placement in a Three-Dimensional Integrated Circuit Employing Distributed Through-Silicon-Via Farms," **US Patent 9,626,311.**

5. Sung Kyu Lim, Kambiz Samadi, and Yang Du, "Power Delivery Network Design for Monolithic Three Dimensional Integrated Circuit," US Patent Pending **US Patent 9,741,691.**

6. Sung Kyu Lim, Ratibor Radojcic, and Yang Du, "Through-Silicon Via (TSV) Crack Sensors for Detecting TSV Cracks in Three-dimensional Integrated Circuits and Related Methods and Systems," **US Patent 9,869,713.**

7. Sung Kyu Lim, Kambiz Samadi, Pratyush Kamal, and Yang Du, "High Quality Physical Design for Monolithic Three-Dimensional Integrated Circuits Using Two-Dimensional Integrated Circuit Design Tools," US Patent Pending.

8. Sung Kyu Lim, Francois Atallah, Rashid Attar, Keith Bowman, Yang Du, Juzer Fatehi, Jai Kumar, Yu Pu, Giby Samson, and Kendrick Yuen, "Clock Tree Design Method for Ultra-Wide Voltage Range Circuits," US Patent Pending.

5.5 Presentations

5.5.1 Invited Keynote Talks

1. "Electrical Design, Modeling & Characterization for 3D Package," Samsung Future Technology Forum, Hwasung, March 28, 2012. **KEYNOTE SPEECH.**
2. "3D IC Design and CAD Research: Challenges and Opportunities," Design, Automation, and Test in Europe (DATE), Workshop on 3D Integration, Grenoble, France. Invited by Prof. Qiang Xu. March 22, 2013. **KEYNOTE SPEECH.**
3. "Modeling, Design, and EDA Research for Stacked-Die 3D IC at GTCAD Lab," International SoC Design Conference (ISOCC), Jeju, Korea. Invited by Prof. Jun Rim Choi. November 5, 2014. **KEYNOTE SPEECH.**
4. "Opportunities and Challenges of 3D ICs in Space Computing," Fault-Tolerant Spaceborne Computing Employing New Technologies, Albuquerque, NM. Invited by Larry Bergman. May 27, 2015. **KEYNOTE SPEECH.**
5. "Going 3D for the Next Generation Designs: New Benefits, Challenges, and Tool Needs," Cadence Summit, San Jose, CA. Invited by Dr. Patrick Hasper, December 10, 2015. **KEYNOTE SPEECH.**
6. "Device, Chip, and Package Co-Optimization for Future 3D IC Memory and Logic Products," International Sandisk Technology Conference, Milpitas, CA. Invited by Dr. Suresh Upadhyayula, March 8, 2016. **KEYNOTE SPEECH.**
7. "Emerging Trends in Heterogeneous System Integration Using 2.5D and 3D IC Technologies," International Conference on Smart Media and Applications, Salamanca, Spain. Invited by Prof. Jin-Gwang Koh, June 25, 2018. **KEYNOTE SPEECH.**
8. "Machine Learning-Powered VLSI Physical Design Tools and Methodologies," Product Enablement Solution Group, AI CAD Workshop, Intel Corporation. Invited by Dr. Harald Gossner (Intel), November 2, 2020. **KEYNOTE SPEECH.**
9. "Electronic Design Automation Needs and Status for Die-Stacked Digital 3D Integrated Circuits," Intel Future Integrated Systems and Technologies Summit (iFISTs). Invited by Dr. Joshua Fryman (Intel), November 3, 2022. **KEYNOTE SPEECH.**
10. "Glass Interposer Integration of Logic and Memory Chiplets: PPA and Reliability Benefits," International Symposium on Microelectronics and Packaging. Invited by Dr. Kwang-Seong Choi (ETRI), November 10, 2022. **KEYNOTE SPEECH.**
11. "Machine Learning-Powered VLSI Physical Design Automation," IEEE Electronic Design Process Symposium. Invited by Dr. Chris Cheng (HP), October 5, 2023. **KEYNOTE SPEECH.**
12. "Quantified Benchmarking: A Key Role of Electronic Design Automation in Heterogenous Integration Era," Qualcomm Core PPA Optimization (QCPO) Summit. Invited by the QCPO Committee, November 7, 2023. **KEYNOTE SPEECH.**

5.5.2 Invited Tutorials

1. "3D IC and TSV Reliability: What Are the Burning Issues and Their Potential Solutions?" *IEEE/ACM Asia South Pacific Design Automation Conference (ASPDAC)*, Sydney, Australia. January 30, 2012.
2. "System-level Design and Analysis for Thermo-Electro-Mechanical Reliability in Through-Silicon-Via Based 3D ICs," *IEEE International Reliability Physics Symposium (IRPS)*, Anaheim, USA. April 15, 2012.

3. "Design of 3D ICs: From Concept to Practice," *IEEE International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, USA. March 4, 2013.

4. "Design for Monolithic 3D IC," *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, San Francisco, USA. October 6, 2014.

5. "How To Build Irresistible 3D IC Physical Layouts: Tools, Methodologies, and Case Studies," *ACM Design Automation Conference*, Austin, USA. June 7, 2016.

6. "Design and CAD Research for Monolithic 3D ICs: Recent Advancement," *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, San Francisco, USA. October 11, 2016.

7. "State-of-the-Art in RTL-to-GDS Tools for Monolithic 3D ICs," *ACM Design Automation Conference*, Las Vegas, USA. June, 2019.

5.5.3 Invited Panels

1. "3D IC: Advanced Packaging Beyond Chiplets," *Chiplets for HPC and Advanced Sensors Workshop*, Chaired by John Shalf. Berkeley, USA. August 15, 2023.

2. "Panel on Multi-die Heterogenous Integration," *IEEE Electronic Design Process Symposium*, Chaired by Shankar Hemmady. San Jose, USA. October 5, 2023.

3. "IEEE EPS and CEDA Joint Panel on Co-Design for AI," *IEEE International Microsystems, Packaging, Assembly and Circuits Technology Conference*, Chaired by CP Hung. Taipei, Taiwan. October 26, 2023.

5.5.4 Invited Conference & Workshop Talks

1. "Thermal/Power-Aware Physical Design for 3D ICs," Georgia Institute of Technology, Atlanta. Invited by Prof. Paul Kohl. May 7, 2007.

2. "Co-Optimization and Limit Study of Signal, Power, and Thermal Distribution Networks in 3D ICs," Georgia Institute of Technology, Atlanta. Invited by Prof. Paul Kohl. August 28, 2008.

3. "Co-Optimization and Limit Study of Signal, Power, and Thermal Distribution Networks in 3D ICs," Workshop on Integrated CAD Tools for Next Generation Thermal Management Methodologies and Devices: Status and Needs, Georgia Institute of Technology, Atlanta. Invited by Prof. Paul Kohl. November 17, 2008.

4. "3D VLSI Design with Through-Silicon-Via: Challenges and Opportunities," Electronic Design Processes (EDP) Symposium Workshop, Monterey. Invited by Dr. Dwight Hill. April 9, 2010.

5. "Designing Future 3D ICs: Benefits and Challenges," First Workshop on 3D Integration, Focus Center Research Program (FCRP). On-line. Invited by Dr. Paul Kohl. February 11, 2011.

6. "Design Tradeoff Studies for the 3D Integration in Extreme Scale," Second Workshop on 3D Integration, Focus Center Research Program (FCRP). On-line. Invited by Dr. Paul Kohl. March 10, 2012.

7. "Design for Electro-Thermo-Mechanical Reliability in 3D ICs," DAC Workshop on More than Moore Technologies, San Francisco. Invited by Dr. Rasit Topaloglu. June 3, 2012.

8. "Teaching Example: A Decade of Physical Design," Young Faculty Workshop at DAC, San Francisco. Invited by Dr. Soha Hassoun. June 3, 2012.

9. "CAD Tool and Methodology for Reliable 3D-IC Integration," GRC Technology Transfer e-Workshop, Semiconductor Research Corporation. Invited by Dr. William Joyner. July 18, 2013.

10. "3D Modeling and Tools," Advanced Metallization Conference, Albany, NY. Invited by Dr. Rajiv Joshi. October 22, 2013.

11. "Low Power Computing with Multi-core 3D Processors," GRC Technology Transfer e-Workshop, Semiconductor Research Corporation. Invited by Dr. David Ye. February 21, 2014.
12. "EDA for Monolithic 3D IC," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), San Francisco. Invited by Zvi Or Bach. October 7, 2014.
13. "3D VLSI: Challenges and Opportunities," The MINOS LabEx Workshop, Grenoble, France. Invited by Dr. Olivier Joubert. March 16, 2015.
14. "2D IC vs. TSV 3D IC vs. Monolithic 3D IC Comparisons," Coolcube Workshop, Qualcomm, San Diego. Invited by Dr. Yang Du. December 4, 2015.
15. "Design and CAD Research for Monolithic 3D ICs," International Conference on Electronic Materials and Nanotechnology for Green Environment (ENGE), Jeju, South Korea. Invited by Prof. Rino Choi. November 9, 2016.
16. "Recent Advancement of RTL-to-GDS Toolset for Monolithic 3D ICs," 3DVLSI Workshop, San Francisco. October 16, 2018.
17. "Micro-bumping vs. Hybrid Bonding: 3D IC PPA and Reliability Comparisons," IEEE International 3D System Integration Conference (3DIC), Raleigh, North Carolina. Invited by Prof. Paul Franzon. November 15, 2021.
18. "EDA Tools and PPA Tradeoff Studies for Micro-bump and Hybrid Bond 3D ICs," DATE Conference Workshop on 3D Integration: Heterogeneous 3D Architectures and Sensors. Invited by Dr. Pascal Vivet. March 18, 2022.
19. "Micro-bumping vs. Hybrid Bonding: What Are the Pros and Cons Today and In the Future?" International Symposium on 3D IC and Heterogeneous Integration. Invited by Prof. Tim Cheng, The Hong Kong University of Science and Technology (HKUST). April 26, 2022.
20. "Machine Learning-Powered VLSI Physical Design Tools and Methodologies," ACM Design Automation, Engineering Track Talk. Invited by Dr. Sabya Das (Synopsys), July 12, 2022.
21. "Glass Interposer Integration of Logic and Memory Chiplets: PPA and Reliability Benefits," International Conference on Electronic Materials and Nanotechnology for Green Environment (ENGE), Jeju, South Korea. Invited by Prof. Hyun Yong Yu. November 9, 2022.

5.5.5 Invited Seminar Presentations at Universities

1. "Physical Design Automation for Fast and Reliable 3D Circuits," Princeton University. Invited by Prof. Sharad Malik. May 3, 2006.
2. "Physical Design Automation for Fast and Reliable 3D Circuits," University of Texas, Austin. Invited by Prof. David Pan. March 29, 2007.
3. "Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory," National Taiwan University (NTU). Invited by Prof. Yao-Wen Chang. June 9, 2010.
4. "Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory," National Chiao Tung University (NCTU). Invited by Prof. Hung-Ming Chen. June 11, 2010.
5. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," Columbia University. Invited by Prof. Ken Shepard. September 17, 2013.
6. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," Massachusetts Institute of Technology. Invited by Prof. Li-Shiuan Peh and Prof. Vivienne Sze. September 27, 2013.
7. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," Harvard University. Invited by Prof. Vahid Tarokh. October 4, 2013.
8. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," California Institute of Technology. Invited by Prof. Azita Emami. October 11, 2013.

9. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," University of California, San Diego. Invited by Prof. Andrew Kahng. October 14, 2013.
10. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," Stanford University. Invited by Prof. Subhasish Mitra. November 5, 2013.
11. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," University of California, Berkeley. Invited by Prof. Elad Alon. November 8, 2013.
12. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," Princeton University. Invited by Prof. Sharad Malik. November 12, 2013.
13. "3D IC Revolution: Where Are We Now, and What Is Next?" Nanyang Technological University, Singapore. Invited by Prof. Hao Yu. November 8, 2016.
14. "Heterogeneous 3D ICs: Benefits, Challenges, and Future Prospects," Southern University of Science and Technology, China. Invited by Prof. Hao Yu. November 8, 2016. May 13, 2019.
15. "Heterogeneous 3D ICs: Benefits, Challenges, and Future Prospects," UCLA. Invited by Prof. Jason Cong. October 11, 2019.
16. "Heterogeneous Integration with 3D ICs: Benefits, Challenges, and Physical Design Tools," UCSD. Invited by Prof. Andrew Kahng. February 23, 2021.
17. "Heterogeneous Integration with 3D ICs: Benefits, Challenges, and Physical Design Tools," UCSD. Invited by Prof. Mingu Kang. March 1, 2022.
18. "Micro-bumping vs. Hybrid Bonding: 3D IC PPA and Reliability Comparisons," University of Notre Dame. Invited by Prof. Ningyuan Cao, March 4, 2022.
19. "Quantified Benchmarking: A Key Role of Electronic Design Automation in Heterogenous Integration Era," Charles L. and Ann Lee Brown Distinguished Seminar Series, University of Virginia. Invited by Prof. Mona Zebarjadi, October 20, 2023.
20. "Quantified Benchmarking: A Key Role of Electronic Design Automation in Heterogenous Integration Era," National Taiwan University. Invited by Prof. Yao-Wen Chang, October 23, 2023.
21. "Quantified Benchmarking: A Key Role of Electronic Design Automation in Heterogenous Integration Era," National Yang Ming Chiao Tung University. Invited by Prof. Hung-Ming Chen, October 24, 2023.
22. "Quantified Benchmarking: A Key Role of Electronic Design Automation in Heterogenous Integration Era," Mercer Distinguished Lecture Series, Rensselaer Polytechnic Institute. Invited by Prof. Liu Liu, November 7, 2023.
23. "Quantified Benchmarking: A Key Role of Electronic Design Automation in Heterogenous Integration Era," ECE Graduate Seminar, University of Pittsburgh. Invited by Prof. Inhee Lee, March 6, 2024.

5.5.6 Invited Seminar Presentations at Industry

1. "Physical Design Automation for Emerging Technologies," Xilinx Corporation, San Jose, USA. Invited by Dr. Amit Singh. November 10, 2003.
2. "Physical Design Automation for Fast and Reliable 3D Circuits," Intel Corporation, Santa Clara, USA. Invited by Dr. Jeff Parkhurst. August 23, 2006.
3. "High Performance 3D Microarchitecture Design," IBM T. J. Watson Research Center, Yorktown Heights, USA. Invited by Dr. Joel Silberman. October 3, 2007.
4. "Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory," Synopsys Corporation, Sunnyvale, USA. Invited by Dr. Jamil Kawa. November 2, 2009.

5. "3D VLSI Design with Through-Silicon-Via: Challenges and Opportunities," Intel Corporation, Santa Clara, USA. Invited by Dr. Rajiv Mathur. November 3, 2009.
6. "3D VLSI Design with Through-Silicon-Via: Challenges and Opportunities," GlobalFoundries, Sunnyvale, USA. Invited by Dr. Rasit Topaloglu. November 3, 2009.
7. "Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory," TSMC, Hsinhsu, Taiwan. Invited by Dr. Kevin Wu. June 10, 2010.
8. "Exploiting the Long-term Advantages of 3D Integration: A Benefit and Limit Study," Intel Corporation, Hillsboro, USA. Invited by Dr. Rajiv Mathur. September 1, 2010.
9. "Architecture and Design Research Activities for 3D ICs at the Georgia Tech Computer-Aided Design Laboratory," Raytheon Corporation, Dallas, USA. Invited by Dr. Kelly Dodds. April 27, 2011.
10. "Designing with TSVs: What to Do and What Not to Do," Institute of Microelectronics, A-STAR, Singapore. Invited by Dr. Min Kyu Je. August 4, 2011.
11. "3D IC Design and CAD Research at GTCAD Laboratory," IBM T. J. Watson Research Center, Yorktown Heights, USA. Invited by Dr. Jeonghee Shin. January 9, 2012.
12. "3D IC Design and CAD Research at GTCAD Lab," Qualcomm Corporation, San Diego, USA. Invited by Dr. Kambiz Samadi. February 10, 2012.
13. "3D IC Design and CAD Research Activities at GTCAD Laboratory," Cadence Design Systems, San Jose, USA. Invited by Dr. Limin He. November 9, 2012.
14. "3D IC Design and CAD Research at GTCAD Laboratory," Fujitsu Corporation, Kawasaki, Japan. Invited by Dr. Toshiyuki Shibuya, January 11, 2013.
15. "Design and CAD Research for Monolithic 3D ICs at GTCAD Lab," CEA-LETI, Grenoble, France. Invited by Dr. Carlo Reita, March 22, 2013.
16. "Physical Design Tools for 3D ICs at GTCAD Lab," Cadence Design Systems, Shanghai, China. Invited by Dr. Tao Chen, September 2, 2013.
17. "Power, Performance, and Thermal Tradeoff Study for Ultra-High Density Monolithic 3D IC Designs," Qualcomm Corporation, San Diego, USA. Invited by Dr. Kambiz Samadi. October 15, 2013.
18. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," Synopsys Corporation, Sunnyvale, USA. Invited by Dr. Arthur Nieuwoudt. November 20, 2013.
19. "Parasitic Extraction and Optimization for TSV-based 3D ICs," Mentor Graphics, Fremont, USA. Invited by Dr. Dusan Petranovik. November 21, 2013.
20. "Physical Design Tools for 3D ICs at GTCAD Lab," Cadence Design Systems, San Jose, USA. Invited by Dr. Limin He. November 22, 2013.
21. "Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory," Altera Corporation, San Jose, USA. Invited by Dr. Arif Rahman, June 4, 2014.
22. "Modeling, Design, and EDA Research for Monolithic 3D ICs," Qualcomm Research, San Diego, USA. Invited by Dr. Yang Du. August 5, 2014.
23. "Modeling, Design, and EDA Research for Stacked-Die 3D IC at GTCAD Lab," ARM Research, Austin, USA. Invited by Dr. Saurabh Sinha. August 21, 2014.
24. "Modeling, Design, and EDA Research for Stacked-Die 3D IC at GTCAD Laboratory," TSMC, Hsinchu, Taiwan. Invited by Dr. Hsien-Hsin Lee. January 12, 2015.
25. "Recent Advances in 3D IC Design Study and CAD Tool Development," GlobalFoundries, Santa Clara, USA. Invited by Dr. Deepak Nayak. June 9, 2015.

26. "New Developments in 3D IC Design and CAD Research at the GTCAD Laboratory," IMEC, Leuven, Belgium. Invited by Dr. Praveen Raghavan. July 27, 2015.

27. "New Developments in 3D IC Design and CAD Research at the GTCAD Laboratory," CEA-LETI, Grenoble, France. Invited by Dr. Fabien Clermidy. November 24, 2015.

28. "3D IC Revolution: Where Are We Now, and What Is Next?," ARM Research Summit, Cambridge, UK. September 16, 2016.

29. "How to Use Commercial 2D IC EDA Tools to Build Commercial Quality Monolithic 3D IC Designs," CEA-LETI, Grenoble, France. Invited by Dr. Pascal Vivet. June 26, 2017.

30. "Emerging Trends in Heterogeneous System Integration Using 3D IC Technologies," Jet Propulsion Laboratory, Pasadena. Invited by Dr. Jean Yang-Scharlotta, May 10, 2018.

31. "Machine Learning to Predict Successful FPGA Compilation Strategy," Intel, Santa Clara. Invited by Dr. Hong Wang. October 15, 2018.

32. "Heterogeneous 2.5D and 3D ICs: Benefits, Challenges, and Future Prospects," ASTAR-IME, Singapore. Invited by Dr. Kuang Kuo Lin, August 16, 2019.

33. "RTL-to-GDS Tool Development for 3D ICs," Synopsys, Mountain View. Invited by Dr. Brandon Wang. September 12, 2019.

34. "Heterogeneous 3D ICs: Benefits, Challenges, and Future Prospects," ARM Research Summit, Austin. Invited by Dr. Saurabh Sinha, September 17, 2019.

35. "Heterogeneous 3D ICs: Benefits, Challenges, and Future Prospects," Northrop Grumman, Redondo Beach. Invited by Dr. Prakash Sarathy, October 10, 2019.

36. "Machine Learning-Powered VLSI Physical Design Tools and Methodologies," Google. Invited by Dr. Azalia Mirhoseini, September 23, 2020.

37. "Machine Learning-Powered VLSI Physical Design Tools and Methodologies," Apple. Invited by Dr. Ajay Bhatia, October 22, 2020.

38. "Machine Learning-Powered VLSI Physical Design Tools and Methodologies," Intel. Invited by Dr. Harald Gossner, November 3, 2020.

39. "Machine Learning-Powered VLSI Physical Design Tools and Methodologies," Nvidia. Invited by Dr. Mark Ren, August 13, 2021.

40. "Machine Learning-Powered VLSI Physical Design Tools and Methodologies," Intel. Invited by Dr. Desmond Kirkpatrick, October 20, 2021.

41. "Machine Learning-Powered VLSI Physical Design Tools and Methodologies," Intel Grow with Technology Series. Invited by Dr. Dhanapathy Krishnamoorthy, March 15, 2022. (260 on-line attendees from Intel)

42. "Micro-Bumping vs. Hybrid Bonding: 3D IC PPA and Reliability," Apple. Invited by Dr. Ajay Bhatia, April 1, 2022.

43. "Micro-Bumping vs. Hybrid Bonding: 3D IC PPA and Reliability," Intel. Invited by Dr. Sonia Leon, April 4, 2022.

44. "Quantified Benchmarking: A Key Role of Electronic Design Automation in Heterogenous Integration Era," TSMC. Invited by Dr. Jim Chang, October 25, 2023.

45. "Unlocking the Future: Designing next generation AI Chips with AI Algorithms," Samsung Semiconductor. Invited by Cas Licari, October 15, 2024.

5.5.7 Invited Seminar Presentations at Korean Industry and Institutes

1. "Multi-level Optimization Techniques for the Physical Design Automation of VLSI Systems," Samsung Semiconductor, Kiheung. Invited by Dr. Kyu Myoung Choi at CAE Team, July 19, 2001.
2. "Physical Design for 3D Integration at the Chip and Package Level," LG Mobile Handset R&D Center, Seoul. Invited by Dr. Soo Youl Yang, July 6, 2007.
3. "Physical Design for 3D Integration at the Chip and Package Level," Samsung Semiconductor, Kiheung. Invited by Dr. Kyu Myoung Choi at System LSI Team, July 11, 2007.
4. "3D Integrated Circuits: Challenges and Opportunities," Hynix Semiconductor Inc., Icheon. Invited by Dr. Jun Ho Lee at Memory R&D Division, January 24, 2008.
5. "Power and Thermal-aware Architecture, Circuits, and Interconnect Techniques," Samsung Semiconductor, Kiheung. Invited by Dr. Jin Suk Kong at System LSI Team, June 3, 2008.
6. "Co-Optimization and Limit Study of Signal, Power, and Thermal Distribution Networks in 3D ICs," Electronics and Telecommunications Research Institute (ETRI), Kwangju, Invited by Dr. Hyun Suh Kang, December 11, 2008.
7. "Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory," Samsung Semiconductor, Kiheung. Invited by Dr. Kyu Myoung Choi at System LSI Team, June 3, 2010.
8. "Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory," Electronics and Telecommunications Research Institute (ETRI), Daejon. Invited by Dr. Gwang Sung Choi, June 7, 2010.
9. "Through-Silicon-Via based 3D IC Research Activities At the Georgia Tech Computer-Aided Design Laboratory," Samsung Semiconductor, Kiheung. Invited by Dr. Tae Je Cho at System LSI Team, June 17, 2010.
10. "Designing with TSVs: What to Do and What Not to Do," Samsung Electronics, Hwasung. Invited by Dr. Chan-Seok Hwang, CAE Team, Memory Division, May 11, 2011.
11. "Designing with TSVs: What to Do and What Not to Do," Hynix Semiconductor Inc., Icheon. Invited by Dr. Jun Ho Lee, Memory R&D Division, August 8, 2011.
12. "Designing with TSVs: What to Do and What Not to Do," Samsung Electronics, Kiheung, Invited by Dr. Ki Sup Kim, Design Technologies, August 9, 2011.
13. "Design and Testing for 3D-MAPS VLIW 3D Processors," Samsung Advanced Institute of Technology, Kiheung. Invited by Dr. Min Woo Ahn, August 3, 2013.
14. "Design Solutions for Multi-Physics Reliability Issues in 3D ICs," Samsung Electronics, Hwasung. Invited by Dr. Chan-Seok Hwang, CAE Team, Memory Division, January 15, 2014.
15. "New Developments in Design and CAD Research for the Current and Future 3D ICs," Samsung Electronics, Hwasung. Invited by Dr. Younsik Park, Design Team, Memory Division, August 31, 2015.
16. "3D IC Revolution: Where Are We Now, and What Is Next?" Korean Institute of Science and Technology (KIST), Seoul, Korea. Invited by Dr. Hyung Joon Kim, November 10, 2016.
17. "Mobile Deep Learning with 3D ICs: Opportunities and Challenges" Electronics and Telecommunications Research Institute (ETRI), Daejon, Korea. Invited by Dr. Young Soo Kwon, January 5, 2017.
18. "Emerging Trends in Heterogeneous System Integration Using 2.5D and 3D IC Technologies," Electronics and Telecommunications Research Institute (ETRI), Daejon, Korea. Invited by Dr. Kwang-Seong Choi, June 4, 2018.

19. "Emerging Trends in Heterogeneous System Integration Using 2.5D and 3D IC Technologies," Samsung Electronics, Chonan, Korea. Invited by Dr. Dong Wook Kim, June 5, 2018.
20. "3D ICs: Benefits, Challenges, and Future Prospects," Samsung Electronics, Hwasung. Invited by Dr. Byunghak Cho, Samsung System LSI, May 10, 2021.
21. "Machine Learning-Powered VLSI Physical Design Tools and Methodologies," Samsung System LSI, Invited by Dr. Byunghak Cho, May 13, 2021.
22. "Design Technologies for Advanced Packages," IEIE Advanced Packaging Technology Workshop, Invited by Prof. Byunghoon Lee, POSTECH, September 24, 2021.
23. "3D ICs: Benefits, Challenges, and Future Prospects from Designer's Perspective," IEIE Semiconductor Industry University Collaboration Workshop. Invited by Prof. Byunghoon Lee, POSTECH, October 27, 2021.
24. "Glass Interposer Integration of Logic and Memory Chiplets: PPA and Power/Signal Integrity Benefits," Electronics and Telecommunications Research Institute (ETRI), Daejon, Korea. Invited by Dr. Young Soo Kwon, September 1, 2022.
25. "Micro-bumping vs. Hybrid Bonding: Pros/Cons in Terms of Power Delivery," Samsung Electronics Fellow and Master Group, Invited by Dr. Sung Wook Moon, September 16, 2022.
26. "Power Delivery Network Design for 3D ICs: Challenges and Solutions," IEIE Semiconductor Industry University Collaboration Workshop. Invited by Prof. Hi-Deok Lee, Chungnam National University, October 5, 2022.
27. "Unlocking the Future: Designing next generation AI Chips with AI Algorithms," Korea Advanced Institute of Science & Technology (KAIST), Daejon, Korea. Invited by Dr. Myung Soo Jung, October 21, 2024.

6 Service

6.1 Professional Contributions

6.1.1 Editorial Board

1. Associate Editor, *IEEE Design & Test* (2015–present)
2. Associate Editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2013–2018)
3. Associate Editor, *IEEE Transactions on Very Large Scale Integration Systems* (2007–2009)
4. Guest Editor, *ACM Transactions on Design Automation of Electronic Systems*, "Special Issue on Demonstrable Software Systems and Hardware Platforms" (2006)
5. Guest Editor, *International Journal of Computational Science and Engineering*, "Special Issue on Computational Methods and Techniques for Nanoscale Technology Computer Aided Design" (2007)
6. Guest Editor, *IEEE Design & Test*, "Special Issue on Advances in 3D Integrated Circuits, Systems, and CAD Tools" (2015)

6.1.2 Technical Program Committee

1. **ACM Design Automation Conference (DAC): 2011, 2012, 2013, 2014, 2017, 2018**
2. **IEEE International Conference on Computer-Aided Design (ICCAD): 2009, 2010, 2014 (track chair), 2015 (track chair), 2016 (track chair), 2022, 2023**
3. IEEE International 3D System Integration Conference (3DIC): 2010, 2011, 2013, 2014, 2015, 2018, 2019

4. International Symposium on Low Power Electronics and Design (ISLPED): 2016, 2017, 2018, 2020, 2021
5. Design, Automation, and Test in Europe (DATE): 2013
6. ACM International Symposium on Physical Design (ISPD): 2006, 2007, 2025
7. IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S): 2019
8. IEEE International Symposium on Quality Electronic Design (ISQED): 2016 (track chair), 2017 (track chair)
9. ACM/IEEE Asia South Pacific Design Automation Conference (ASPDAC): 2005, 2008, 2009, 2013
10. ACM/IEEE System Level Interconnect Prediction: 2011
11. IEEE International Symposium on Circuits and Systems: 2002, 2003
12. ACM Great Lakes Symposium on VLSI: 2004, 2005, 2006, 2007
13. IEEE International Conference on Computer Design: 2003, 2005, 2006, 2007
14. IFIP/IEEE International Conference on VLSI-SoC: 2004, 2007, 2011, 2012
15. International Conference on Parallel Processing: 2005

6.1.3 Professional Membership

1. Institute of Electrical and Electronics Engineers (IEEE), member (1995–2005), senior member (2006–2022), fellow (2023–present) for "contributions to electronic design automation and tradeoff for 3-dimensional integrated circuits,"
2. Association for Computing Machinery (ACM), member (1995–present)
3. Advisory Board Member, ACM Special Interest Group on Design Automation (SIGDA) (2003–2007)
4. Proposal Review Panel: National Science Foundation (NSF), CISE/CCF Division (March 29-30, 2012)
5. ACM/SIGDA Outstanding PhD Dissertation in EDA Award (OPDA) Selection Committee (2013)
6. Panel Chair (2012), Finance Chair (2013), Technical Program Committee Chair (2014), ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)
7. Publication Chair (2005) and Tutorials Chair (2006), International Conference on Compilers, Architectures and Synthesis of Embedded Systems
8. CAD Track Chair, IEEE International Symposium on Circuits and Systems (2004–2006)
9. Publication Chair, IFIP International Conference on VLSI (2007)
10. Co-chair, Workshop on Accelerating Time-to-Market through Compiler-driven Optimization of Embedded Platforms (2004)

6.1.4 Invited Special Sessions and Panels Organized

1. Organizer, "Killer Apps for 3D ICs?" Special Session, ACM Design Automation Conference (DAC), 2011.
2. Tutorial Organizer, "How To Build Irresistible 3D IC Physical Layouts: Tools, Methodologies, and Case Studies," ACM Design Automation Conference (DAC), 2016.
3. Organizer, "Negative Capacitance Field Effect Transistors (NCFET) for Ultra-Low-Power Devices to Systems," Special Session, ACM Design Automation Conference (DAC), 2018.
4. Organizer, "Monolithic 3D IC: Benefits, Architectures, and EDA Tools," Special Session, ACM Design Automation Conference (DAC), 2019.
5. Organizer, "Heterogenous 3D or Monolithic 3D, Which Direction to Go?" Panel, ACM Design Automation Conference (DAC), 2022.

6.1.5 Professional Leadership

1. Theme Leader, Semiconductor Research Corporation (SRC), Focus Center Research Program (FCRP): Cross-Center Research in 3D Integration (2009 – 2012)
2. Organizer, "Opportunities and Challenges in Emerging High-Performance Heterogeneous 3D Systems," First Annual Workshop, Cross-center Theme on 3D Integration, Focus Center Research Program (FCRP) of the Semiconductor Research Corporation (SRC), February 11, 2011. 300+ registrants, open to public.
3. Organizer, "3D Integration: Progress and Prospects," Second Annual Workshop, Cross-center Theme on 3D Integration, Focus Center Research Program (FCRP) of the Semiconductor Research Corporation (SRC), March 9, 2012. 235 registrants, closed to FCRP members only.
4. Member, International Technology Roadmap for Semiconductors (ITRS): Design International Technology Working Group for the 2009 renewal of ITRS.
5. Founding Coordinator, Dual BS/MS Program between GT-ECE and KAIST-EE (Korean Advanced Institute of Science and Technology) (2008–)
6. Advisory Board member, MonolithIC 3D, Inc. (2013–2015)

6.1.6 Literature Review

1. Journal articles
    - *ACM Transactions on Design Automation of Electronic Systems*
    - *ACM Journal of Emerging Technologies in Computing*
    - *IEEE Design & Test of Computers*
    - *IEEE Journal of Solid-State Circuits*
    - *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*
    - *IEEE Transactions on Very Large Scale Integration Systems*
    - *IEEE Transactions on Components, Packaging and Manufacturing Technology*
    - *IEEE Transactions on Device and Materials Reliability*
    - *IEEE Transactions on Circuits and Systems*
    - *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*
2. Conference papers
    - ACM Design Automation Conference (DAC)
    - ACM International Symposium on Physical Design (ISPD)
    - ACM Great Lakes Symposium on VLSI (GLS-VLSI)
    - ACM System Level Interconnect Prediction (SLIP)
    - IEEE International Conference on Computer-Aided Design (ICCAD)
    - IEEE International Symposium on Circuits and Systems (ISCAS)
    - IEEE International Conference on Computer Design (ICCD)
    - IEEE Asia South Pacific Design Automation Conference (ASPDAC)
    - IEEE Design Automation & Test in Europe (DATE)
    - IEEE International Symposium on Low Power Electronics and Design (ISLPED)
    - IEEE International 3D System Integration Conference (3DIC)

6.2 Campus Contributions

1. Member, Graduate Curriculum Committee, School of Electrical and Computer Engineering (2002 – 2004)
2. Member, Faculty Honors Committee, School of Electrical and Computer Engineering (2004 – 2007)
3. Member, Undergraduate Curriculum Committee, School of Electrical and Computer Engineering (2007 – 2010)
4. Member, Faculty Recruitment Committee, School of Electrical and Computer Engineering (2010 – 2012)
5. Chair, VLSI Systems and Digital Design Technical Interest Group (2012 – 2015)
6. Member, ECE Statutory Advisory Committee (2015 – present)
7. Member, ECE Peer Review Committee (2017 – present)
8. Faculty advisor, Korean Graduate Student Association (2001 – present)
9. Faculty advisor, Korean Undergraduate Student Association (2001 – present)
10. PhD Committee Service
    (1) Susanta Sengupta: Proposal (spring 2002)
    (2) Sidharth Dalmia: Proposal (fall 2002)
    (3) Kyu Won Choi: Proposal (fall 2002), Defense (fall 2003)
    (4) Eung Suh Shin: Proposal (spring 2003), Defense (fall 2003)
    (5) Prateek Tandon: Proposal (spring 2004)
    (6) Badri Varadarajan: Proposal (fall 2003)
    (7) William Robinson: Defense (fall 2003)
    (8) Jifeng Mao: Proposal (fall 2003), Defense (fall 2004)
    (9) Chung Seok Seo: Proposal (fall 2003)
    (10) Sung-Hwan Min: Proposal (fall 2003), Defense (spring 2004)
    (11) Sandeep Sankararaman: Proposal (fall 2003)
    (12) Jae Hwan Lee: Proposal (spring 2004), Defense (fall 2004)
    (13) Mongkol Ekpanyapong: Proposal (spring 2005), Defense (fall 2005)
    (14) Ajay Joshi: Proposal (spring 2005), Defense (spring 2006)
    (15) Bing Dang: Proposal (summer 2005), Defense (summer 2006)
    (16) Bhyrav Mutnury: Proposal (summer 2005)
    (17) Pranav Anbalagan: Proposal (fall 2005), Defense (fall 2006)
    (18) Jacob Minz: Proposal (fall 2005), Defense (summer 2006)
    (19) Changsoo Hong: Proposal (fall 2005), Defense (fall 2006)
    (20) Chinnakrishnan Ballapuram: Proposal (spring 2006), Defense (spring 2008)
    (21) Souvik Mukherjee: Proposal (spring 2006), Defense (spring 2007)
    (22) Weidong Shi: Defense (spring 2006)
    (23) Lakshmi Chakrapani: Proposal (summer 2006), Defense (spring 2008)
    (24) Krishna Srinivasan: Proposal (fall 2006), Defense (spring 2008)
    (25) Kiran Puttswamy: Proposal (fall 2006), Defense (fall 2007)
    (26) Faik Baskaya: Proposal (fall 2006), Defense (summer 2009)
    (27) Sudarshan Srinivasan: Defense (summer 2007)
    (28) Ranjeeth Doppalapudi: Proposal (fall 2008)

(29) Seyed-Abdollah Aftabjahani: Proposal (spring 2009), Defense (summer 2011)
(30) Ki Jin Han: Defense (spring 2009)
(31) Nithya Sankaran: Proposal (spring 2010), Defense (spring 2011)
(32) Dong Hyuk Woo: Defense (summer 2010)
(33) Michael Healy: Proposal (spring 2009), Defense (summer 2010)
(34) Tapobrata Bandyopadhyay: Proposal (spring 2011)
(35) Mohit Pathak: Proposal (spring 2011), Defense (spring 2014)
(36) Muhammad Bashir: Proposal (fall 2010), Defense (summer 2011)
(37) Dean Lewis: Proposal (summer 2011), Defense (summer 2012)
(38) Dae Hyun Kim: Proposal (fall 2011), Defense (spring 2012)
(39) Jeremy Tolbert: Proposal (fall 2011), Defense (summer 2012)
(40) Krit Athikulwongse: Proposal (fall 2011), Defense (summer 2012)
(41) Xin Zhao: Proposal (spring 2012), Defense (fall 2012)
(42) Minki Cho: Proposal (spring 2012), Defense (fall 2012)
(43) Nak Hee Seong: Proposal (spring 2012), Defense (summer 2012)
(44) Young Joon Lee: Proposal (spring 2012), Defense (spring 2013)
(45) Calvin King: Defense (spring 2012)
(46) Fahad Ahmed: Proposal (summer 2012)
(47) Jianyong Xie: Proposal (fall 2012), Defense (fall 2013)
(48) Kwanyeob Chae: Proposal (fall 2012), Defense (summer 2013)
(49) Xi Liu: Proposal (fall 2012), Defense (summer 2013)
(50) Shubha Ramakrishnan: Proposal (fall 2012), Defense (spring 2013)
(51) Moongon Jung: Proposal (spring 2013), Defense (spring 2014)
(52) Biancun Xie: Proposal (fall 2013), Defense (fall 2014)
(53) Jiwoo Park (UT Austin): Proposal (fall 2013)
(54) Taigon Song: Proposal (spring 2014), Defense (fall 2015)
(55) Shreepad Panth: Proposal (spring 2014), Defense (spring 2015)
(56) Qiao Chen: Proposal (fall 2014)
(57) Danny Lie: Defense (spring 2015)
(58) William Song: Proposal (spring 2015), Defense (fall 2015)
(59) Sung Joo Park: Proposal (spring 2015), Defense (summer 2016)
(60) Yarui Peng: Proposal (fall 2015), Defense (fall 2016)
(61) Boris Alexandrov: Defense (fall 2015)
(62) Wen Yueh: Defense (fall 2015)
(63) Michelle Collins: Proposal (spring 2016), Defense (fall 2016)
(64) Taizhi Liu: Proposal (spring 2016), Defense (spring 2017)
(65) Sandeep Samal: Proposal (summer 2016), Defense (spring 2017)
(66) Lifeng Nai: Proposal (fall 2016)
(67) Sihwan Kim: Proposal (summer 2017)
(68) Anvesha Amaravati: Proposal (fall 2017), Defense (fall 2018)
(69) Kyung Wook Chang: Proposal (fall 2018), Defense (spring 2019)

(70) Bon Woong Ku: Proposal (fall 2018), Defense (spring 2019)
(71) Huan Yu: Proposal (fall 2018), Defense (fall 2019)
(72) Ningyuan Cao: Proposal (fall 2019), Defense (summer 2020)
(73) Majid Ahadi Dolatsara: Proposal (fall 2019), Defense (spring 2021)
(74) Ningyuan Cao: Proposal (fall 2019)
(75) Xiaoyu Sun: Proposal (fall 2019), Defense (summer 2020)
(76) Venkata Chaitanya Krishna Chekuri: Proposal (spring 2020), Defense (fall 2020)
(77) Anthony Agnesina: Proposal (fall 2020), Defense (spring 2022)
(78) Jinwoo Kim: Proposal (fall 2020), Defense (spring 2022)
(79) Sai Pentapati: Proposal (fall 2020), Defense (spring 2022)
(80) Victor Huang: Proposal (spring 2020), Defense (fall 2021)
(81) Xiaochen Peng: Proposal (spring 2020), Defense (spring 2021)
(82) Hakki Mert Torun: Proposal (spring 2020), Defense (fall 2020)
(83) Osama Waqar Bhatti: Proposal (fall 2021), Defense (fall 2022)
(84) Shanshi Huang: Proposal (fall 2021)
(85) Seunghyup Han: Proposal (fall 2021), Defense (spring 2023)
(86) Yi-chen Lu: Proposal (fall 2021), Defense (spring 2023)
(87) Lingjun Zhu: Proposal (fall 2022), Defense (fall 2023)
(88) Gauthaman Murali: Proposal (fall 2022), Defense (fall 2023)
(89) Pruek Vanna-iampikul: Proposal (spring 2023), Defense (spring 2024)
(90) Mercy Daniel Aguebor: Proposal (fall 2023)
(91) Linhao Yang: Proposal (spring 2024)
(92) Gihun Choe: Defense (fall 2023)
(93) Oluwaseyi Akinwande: : Proposal (fall 2024)
(94) Liu Liu (Univ of Notre Dame): Proposal (fall 2024)
(95) James Read: Proposal (fall 2024)

7 Grants and Contracts

1. Interconnect-centric Physical Design Methodology
    - Role: PI
    - Organization: Georgia Yamacraw
    - Contract Period: August 16, 2001 – August 15, 2004
    - Amount Awarded: $270,000
2. Noise Immune On/Off Chip 3-D Routing for High Speed System-On-Package Substrate
    - Role: PI
    - Organization: National Science Foundation
    - Contract Period: August 15, 2002 – August 14, 2004
    - Amount Awarded: $100,000
3. Chip/Package Co-design of Physical Layout for Fast and Reliable System-On-Packages
    - Role: PI

- Organization: Association for Computing Machinery
- Contract Period: June 15, 2003 – June 14, 2004
- Amount Awarded: $24,000

4. Placement and Routing for Polymorphic Computing Architecture
    - Role: PI
    - Organization: Defense Advanced Research Projects Agency (sub-contract)
    - Contract Period: May 15, 2003 – May 14, 2004
    - Amount Awarded: $45,000
5. NER: Automatic Placement Algorithms for Quantum Cell Automata
    - Role: PI (co-PI: Mike Niemier), my share = $90,813 (70%).
    - Organization: National Science Foundation
    - Contract Period: August 1, 2004 – July 31, 2005
    - Amount Awarded: $129,734
6. Bringing Low Power Reconfigurable Analog Signal Processing to Embedded Systems
    - Role: PI (co-PIs: David Anderson, Paul Hasler), my share = $240,000 (100%).
    - Organization: National Science Foundation
    - Contract Period: September 1, 2004 – August 31, 2007
    - Amount Awarded: $240,000
7. Mixed Signal Design Tool for System-On-Package
    - Role: PI
    - Organization: Packaging Research Center
    - Contract Period: January 8, 2007 – January 7, 2009
    - Amount Awarded: $100,000
8. High-Performance 3D Microarchitecture Design
    - Role: co-PI (co-PIs: Gabriel H. Loh, Hsien-Hsin S. Lee), my share = $70,000 (33%).
    - Organization: Semiconductor Research Corporation (FCRP/GSRC)
    - Contract Period: June 1, 2005 – August 31, 2006
    - Amount Awarded: $210,000
9. High-Performance 3D Microarchitecture Design
    - Role: co-PI (co-PIs: Gabriel H. Loh, Hsien-Hsin S. Lee), my share = $150,000 (33%).
    - Organization: Semiconductor Research Corporation (FCRP/C2S2)
    - Contract Period: September 1, 2006 – August 31, 2009
    - Amount Awarded: $450,000
10. CAREER: Physical Design Automation for Fast and Reliable 3D Circuits
    - Role: PI
    - Organization: National Science Foundation
    - Contract Period: June 15, 2006 – June 14, 2011
    - Amount Awarded: $400,000

11. Co-Optimization and Limit Study of Signal, Power, and Thermal Distribution Networks in 3D ICs
    - Role: PI
    - Organization: Semiconductor Research Corporation (FCRP/IFC)
    - Contract Period: September 1, 2007 – October 31, 2012
    - Amount Awarded: $400,000
12. Design, Fabrication, and Testing of 3D-MAPS: A Massively Parallel Processor with 3D Stacked Memory
    - Role: PI (co-PI: Hsien-Hsin S. Lee), my share = $470,624 (50%).
    - Organization: US Department of Defense
    - Contract Period: May 1, 2009 – September 30, 2011
    - Amount Awarded: $941,248
13. 3D-MAPS V2: A Massively Parallel Processor with 3D Stacked Memory
    - Role: PI (co-PIs: Hsien-Hsin S. Lee), my share = $147,888 (50%).
    - Organization: US Department of Defense
    - Contract Period: October 1, 2011 – September 30, 2012
    - Amount Awarded: $295,776
14. 3D Integration of Sub-Threshold Multi-core Co-processor for Ultra Lower Power Computing
    - Role: PI (co-PI: Saibal Mukhopadhyay), my share = $225,000 (50%).
    - Organization: National Science Foundation
    - Contract Period: August 15, 2009 – August 14, 2012
    - Amount Awarded: $450,000
15. A Digital Infomedia System - Immersive Technologies on a Hybrid GPU-CPU Platform
    - Role: co-PI (co-PIs: Ghassan Al-Regib, Monty Hayes, Fred Juang, Jongman Kim), my share = $254,463 (4.2%).
    - Participating Organizations: Korea Electronics Technology Institute, Kaon Media, Creative Solutions Corporation, Sung-kyun-kwan University, Georgia Tech Enterprise Innovation Institute
    - Organization: Korea Institute for Advancement of Technology, The Ministry of Knowledge Economy, The Republic of Korea
    - Contract Period: March 1, 2009 – February 28, 2012
    - Amount Awarded: $6,000,000
16. Design for Manufacturing Issues with Through-Silicon-Via
    - Role: PI
    - Organization: Intel Corporation
    - Date Awarded: January 2010
    - Amount Awarded: $50,000 (industry gift)
17. High Density 3D SRAM and Logic Designs with Monolithic 3D Integration
    - Role: PI
    - Organization: Semiconductor Research Corporation (Intel Custom Funding)
    - Contract Period: August 1, 2011 – July 31, 2012
    - Amount Awarded: $60,000

18. Reliability and Standardization Study for TSV-based Wide I/O DRAM Structures in 3D-IC Integration
    - Role: PI
    - Organization: Semiconductor Research Corporation (SEMATECH 3D Enablement Center)
    - Contract Period: October 1, 2011 – September 30, 2012
    - Amount Awarded: $59,933
19. Design for Manufacturability of 3D ICs with Through Silicon Vias
    - Role: PI (co-PI: David Pan, UT Austin), my share = $200,000 (50%).
    - Organization: National Science Foundation
    - Contract Period: September 1, 2010 – August 31, 2014
    - Amount Awarded: $400,000
20. Design-for-Yield for future 3D DRAM
    - Role: PI
    - Organization: Samsung Electronics
    - Contract Period: June 15, 2012 – June 14, 2014
    - Amount Awarded: $100,000
21. CAD Tool and Methodology for Reliable 3D-IC Integration
    - Role: co-PI (PI: David Pan, UT Austin), my share = $180,000 (50%).
    - Organization: Semiconductor Research Corporation (GRC/CADTS)
    - Contract Period: February 1, 2012 – August 31, 2015
    - Amount Awarded: $360,000
22. Design of 3D Integrated Heterogeneous Systems
    - Role: co-PI (PI: Saibal Mukhopadhyay), my share = $210,629 (50%).
    - Organization: Semiconductor Research Corporation (GRC/ICSS)
    - Contract Period: Feb 1, 2011 – August 31, 2015
    - Amount Awarded: $421,258
23. Low Power Computing with Multi-core 3D Processors
    - Role: PI
    - Organization: Semiconductor Research Corporation (Intel Custom Funding)
    - Contract Period: April 1, 2012 – March 31, 2015
    - Amount Awarded: $400,000
24. Low Power and Reliable Designs for Monolithic 3D ICs
    - Role: PI
    - Organization: Qualcomm, Inc.
    - Contract Period: August 1, 2012 – July 31, 2015
    - Amount Awarded: $124,000
25. 3D IC Design for Ultra Low Power Wireless Sensor Network
    - Role: PI
    - Organization: Center for Integrated Smart Sensors, KAIST, Korea

- Contract Period: September 1, 2012 – August. 31, 2015
- Amount Awarded: $170,000

26. Architecture-aware Power Distribution Network Design for Wide-I/O 3D DRAM
    - Role: PI
    - Organization: Samsung Electronics
    - Contract Period: December 15, 2013 – December 14, 2015
    - Amount Awarded: $100,000
27. Parasitic Extraction for TSV-based 3D ICs
    - Role: PI
    - Organization: Mentor Graphics
    - Date Awarded: September 2015
    - Amount Awarded: $20,000 (industry gift)
28. Bringing 3D Memory Cubes to Space: a Rad-Hard-by-Design Study with an Open Architecture (SBIR Phase 1)
    - Role: co-PI (PI: James Yamaguchi), my share = $39,000 (31%).
    - Organization: National Aeronautics and Space Administration (NASA)
    - Contract Period: June 1, 2016 – December 31, 2016
    - Amount Awarded: $125,000
29. Power Delivery Network Design and CAD for Monolithic 3D ICs
    - Role: PI
    - Organization: ARM
    - Contract Period: August 1, 2016 – December 31, 2016
    - Amount Awarded: $26,233
30. Next-generation Neuromorphic Co-processor Power Consumption in the Beyond Exa-scale Era
    - Role: PI
    - Organization: Oak Ridge National Laboratory
    - Contract Period: October 1, 2016 – September 30, 2018
    - Amount Awarded: $134,000
31. Exploration of Intrinsic Monolithic 3D IC Design Limits and PPA Analysis
    - Role: PI
    - Organization: Taiwan Semiconductor Manufacturing Company (TSMC)
    - Contract Period: June 1, 2017 – May 31, 2019
    - Amount Awarded: $282,950
32. Bringing 3D Memory Cubes to Space: A Rapid Prototyping Study and Experimental Validation (SBIR Phase 2)
    - Role: co-PI (PI: James Yamaguchi), my share = $200,045 (27%).
    - Organization: National Aeronautics and Space Administration (NASA)
    - Contract Period: June 1, 2017 – June 15, 2020
    - Amount Awarded: $750,000
33. A Vertically-Integrated Design Flow for IP Reuse and Heterogeneous Integration

- Role: PI (co-PI: Saibal Mukhopadhyay, Tushar Krishna, Madhavan Swaminathan), my share = $1,447,400 (39%).
- Organization: Defense Advanced Research Projects Agency (DARPA)
- Contract Period: September 1, 2017 – August 31, 2021
- Amount Awarded: $3,719,691

34. FLASHRAD: A 3D Rad Hard Memory Module For High Performance Space Computers (SBIR Phase 1)
    - Role: co-PI (PI: James Yamaguchi), my share = $38,500 (31%).
    - Organization: National Aeronautics and Space Administration (NASA)
    - Contract Period: June 1, 2017 – December 31, 2017
    - Amount Awarded: $125,000
35. Qualcomm Faculty Award, 2017
    - Role: PI
    - Organization: Qualcomm, Inc.
    - Contract Period: N/A
    - Amount Awarded: $75,000 (industry gift)
36. Device/Circuit Co-design of Negative Capacitance Transistors
    - Role: PI (co-PI: Asif Khan, Georgia Tech), my share = $225,000 (50%)
    - Organization: National Science Foundation
    - Contract Period: September 1, 2017 – August 31, 2022
    - Amount Awarded: $450,000
37. Thermal-aware Tier Partitioning and Extraction for Wafer-bonded 3D ICs
    - Role: PI
    - Semiconductor Research Corporation
    - Contract Period: October 1, 2017 – September 30, 2019
    - Amount Awarded: $130,000
38. Machine Learning to Predict Successful FPGA Compilation Strategy
    - Role: PI
    - Organization: National Science Foundation, Industry-University Cooperative Research Centers (IUCRC) Program
    - Contract Period: January 1, 2018 – December 31, 2019
    - Amount Awarded: $105,000 (overhead 10%)
39. RTL-to-GDS Tools and Methodologies for Sequential Integration Monolithic 3D ICs
    - Role: PI (co-PI: Saibal Mukhopadhyay, Krishnendu Chakrabarty), my share = $1,694,044 (54%).
    - Organization: Defense Advanced Research Projects Agency (DARPA)
    - Contract Period: June 1, 2018 – December 31, 2021
    - Amount Awarded: $3,126,341
40. FLASHRAD: A 3D Rad Hard Memory Module For High Performance Space Computers (SBIR Phase 2)
    - Role: co-PI (PI: James Yamaguchi), my share = $201,102 (27%).

- Organization: National Aeronautics and Space Administration (NASA)
- Contract Period: June 1, 2018 – December 31, 2020
- Amount Awarded: $750,000

41. Qualcomm Faculty Award, 2018

    - Role: PI
    - Organization: Qualcomm, Inc.
    - Contract Period: N/A
    - Amount Awarded: $75,000 (industry gift)

42. Netlist-to-PPA Prediction Using Machine Learning

    - Role: PI
    - Organization: National Science Foundation, Industry-University Cooperative Research Centers (IUCRC) Program
    - Contract Period: January 1, 2019 – December 31, 2019
    - Amount Awarded: $120,000 (overhead 10%)

43. GP-3D: Georgia Tech Placer for True 3D IC Placement

    - Role: PI
    - Organization: Samsung Electronics
    - Contract Period: May 1, 2019 - April 30, 2021
    - Amount Awarded: $150,000

44. Physical Design Tools for Monolithic 3D ICs Targeting Logic Applications

    - Role: PI
    - Organization: Semiconductor Research Corporation
    - Contract Period: January 1, 2020 - December 31, 2023
    - Amount Awarded: $240,000

45. 3D Memory/Logic Stacking Architecture Exploration

    - Role: PI
    - Organization: Interuniversitair Micro-Electronica Centrum (IMEC)
    - Contract Period: March 1, 2021 - February 28, 2025
    - Amount Awarded: $233,903

46. Glass Interposer Integration of Logic and Memory Chiplets: PPA Benefits Over Other Means

    - Role: PI
    - Organization: Facebook via Packaging Research Center (PRC)
    - Contract Period: May 1, 2021 - April 30, 2022
    - Amount Awarded: $70,000

47. Backside Power Delivery Network for 2D and 3D ICs

    - Role: PI
    - Organization: Samsung Semiconductor Inc (San Jose, CA)
    - Contract Period: October 1, 2021 - September 30, 2024

- Amount Awarded: $400,724

48. Abisko: Deep Codesign of an Energy-Optimized, High Performance Neuromorphic Accelerator
    - Role: co-PI (PI: Jeffrey Vetter, Oak Ridge National Lab), my share = $300,000 (5%).
    - Organization: US Department of Energy
    - Contract Period: November 1, 2021 - October 30, 2024
    - Amount Awarded: $6,000,000
49. Power Delivery Network Comparison Between Micro-bump and Hybrid Bonding 3D ICs
    - Role: PI
    - Organization: Samsung Electronics
    - Contract Period: November 1, 2021 - October 31, 2022
    - Amount Awarded: $120,000
50. Physical Design Parameter Optimization (PDPO) Using Reinforcement Learning
    - Role: PI
    - Organization: National Science Foundation, Industry-University Cooperative Research Centers (IUCRC) Program
    - Contract Period: January 1, 2023 – December 31, 2024
    - Amount Awarded: $130,000 (overhead 10%)
51. Enabling Design Space Exploration of Monolithic-3D Logic and Memory Fabrics
    - Role: co-PI (PI: Sharon Hu), my share = $150,000 (33%).
    - Organization: Semiconductor Research Corporation
    - Contract Period: January 1, 2023 - December 31, 2025
    - Amount Awarded: $450,000
52. Design Automation for Monolithic 3D and Heterogeneous Interposer Integration
    - Role: co-PI (PI: Madhavan Swaminathan), my share = $1,250,000 (2.8%).
    - Organization: Semiconductor Research Corporation, Joint University Microelectronics Program 2.0
    - Contract Period: January 1, 2023 - December 31, 2027
    - Amount Awarded: $46,057,763
53. A Multi-tier Fine-Grained 3D Architecture for Efficient Inference and Training of Memory-Intensive AI Workloads
    - Role: co-PI (PI: Tushar Krishna), my share = $150,000 (50%).
    - Organization: Taiwan Semiconductor Manufacturing Company
    - Contract Period: March 15, 2023 - March 14, 2025
    - Amount Awarded: $300,000
54. System-level Evaluation of Monolithic 3D ICs Based on 2D Materials Transistors and Remote Epitaxy
    - Role: PI
    - Organization: Samsung Advanced Institute of Technology (SAIT)
    - Contract Period: November 1, 2023 - October 31, 2025
    - Amount Awarded: $600,000

55. Domain-Specific 3D ReRAM-based Processing-in-Memory Accelerators for Streaming Time Series Applications
    - Role: co-PI (PI: Philip Brisk), my share = $90,000 (22.5%).
    - Organization: National Science Foundation
    - Contract Period: June 6, 2023 - June 5, 2024
    - Amount Awarded: $400,000
56. Routing Design Guided Development of 3D Scaling BEOL Interconnect Technology
    - Role: co-PI (PI: Jae Yong Song), my share = $364,066 (28.5%).
    - Organization: Korea Planning & Evaluation of Industrial Technology (KEIT)
    - Contract Period: April 1, 2023 - December 31, 2027
    - Amount Awarded: $1,275,000
57. ML-based Generation of Fine-grained TSV Models for Power Integrity Analysis
    - Role: PI
    - Organization: National Science Foundation, Industry-University Cooperative Research Centers (IUCRC) Program
    - Contract Period: January 1, 2024 – December 31, 2025
    - Amount Awarded: $145,000 (overhead 10%)
58. AI-based Physical Design Automation for 2D and 3D ICs
    - Role: PI
    - Organization: Samsung Advanced Institute of Technology (SAIT)
    - Contract Period: January 15, 2024 – January 14, 2027
    - Amount Awarded: $856,555
59. Physical Design Closure with Machine Learning
    - Role: PI
    - Organization: Synopsys Corporation
    - Date Awarded: 2021, 2022, 2023, 2024
    - Amount Awarded: $215,000 total (industry gift)

8 Honors and Awards

8.1 Awards

1. Design Automation Conference Graduate Scholarship, 2003.
2. **NSF Faculty Early Career Development (CAREER) Award, 2006.**
3. Outstanding Junior Faculty Member Award, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2007.
4. Hesburgh Award Teaching Fellows, Center for the Enhancement for Teaching and Learning (CETL), Georgia Institute of Technology, 2008. (Institute-level Teaching Award for tenured faculty)
5. Distinguished Service Award, ACM Special Interest Group on Design Automation (SIGDA), 2008.
6. Intel/CICC Student Scholarship Award, IEEE Custom Integrated Circuits Conference (CICC), 2010.

7. Best Paper Award, IEEE Asian Test Symposium, 2012.
8. Best Paper Award, IEEE International Interconnect Technology Conference (IITC), 2014.
9. Best Paper Award, IEEE International Conference on Planarization/CMP Technology (ICPT), 2016.
10. **Class of 1940 Course Survey Teaching Effectiveness Award, 2016. (Institute-level Teaching Award based on Student Course Survey)**
11. Qualcomm Faculty Award, 2017.
12. Best Paper Award, IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS) , 2017.
13. Qualcomm Faculty Award, 2018.
14. **Class of 1940 Course Survey Teaching Effectiveness Award, 2018. (Institute-level Teaching Award based on Student Course Survey)**
15. **Class of 1940 Course Survey Teaching Effectiveness Award, 2019. (Institute-level Teaching Award based on Student Course Survey)**
16. Best Paper Award, IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2020.
17. Best Paper Award, IEEE International Conference on Computer Design (ICCD), 2020.
18. **Class of 1940 Course Survey Teaching Effectiveness Award, 2020. (Institute-level Teaching Award based on Student Course Survey)**
19. Richard B. Shultz Best Paper Award, IEEE Transactions on Electromagnetic Compatibility, 2022.
20. **Donald O. Pederson Best Paper Award, IEEE Transactions on Computer-Aided Design, 2022.**
21. Best Paper Award, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2022.
22. Best Student Paper Award, ACM/IEEE Workshop on Machine Learning for CAD (ML CAD), 2022.
23. **Class of 1940 Course Survey Teaching Effectiveness Award, 2022. (Institute-level Teaching Award based on Student Course Survey)**
24. **Best Paper Award, ACM Design Automation Conference (DAC), 2023.**
25. Award for Excellence, Defense Advanced Research Projects Agency (DARPA), 2024.

8.2 Nominations

1. Best Paper Award nomination, ACM International Symposium on Physical Design (ISPD), 2006.
2. Best Paper Award nomination, IEEE International Conference on Computer-Aided Design (ICCAD), 2009.
3. Best Paper Award nomination, ACM Design Automation Conference (DAC), 2011.
4. Best Paper Award nomination, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2011.
5. Best Paper Award nomination, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2012.
6. Best Paper Award nomination, ACM Design Automation Conference (DAC), 2012.
7. Best Paper Award nomination, IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2012.

8. Best Paper Award nomination, ACM International Symposium on Physical Design (ISPD), 2014.
9. Best Paper Award nomination, ACM Design Automation Conference (DAC), 2014.
10. Best Paper Award nomination, ACM International Symposium on Physical Design (ISPD), 2018.
11. Best Paper Award nomination, IEEE International Conference on Computer-Aided Design (ICCAD), 2019.
12. Best Paper Award nomination, ACM Design Automation Conference (DAC), 2020.
13. Best Paper Award nomination, ACM International Symposium on Physical Design (ISPD), 2021.
14. Best Paper Award nomination, IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2021.
15. Best Paper Award nomination, IEEE International Conference on Computer-Aided Design (ICCAD), 2024.